

# Cool XpressRunner-GS45

## PCI/104-Express CPU Board

### Technical Manual



TME-PCI104E-GS45-R3V1.docx  
Revision 3.1 / December 11

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## ***Technical Manual Cool XpressRunner-GS45***

LiPPERT Document: TME-PCI104E-GS45-R3V1.docx Revision 3.1

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## Acronyms

ACPI	Advanced Configuration and Power Management Interface
AES	Advanced Encryption Standard
APM	Advanced Power Management
ATA	Advanced Technology Attachment
BIOS	Basic Input Output System
BPP	Bits Per Pixel
CD	Compact Disc
COM	Communication Equipment
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CXR	Cool XpressRunner
DAC	Digital-to-Analog-Converter
DDR	Double Data Rate
DMA	Direct Memory Access
DOT	Dynamic Overclocking Technology
EIDE	Enhanced Integrated Device Electronics
EMC	Electromagnetic Compatibility
ETH	Ethernet
FIFO	First In First Out
FPU	Floating Point Unit
FWH	Firmware Hub
GPIO	General Purpose Input Output
HDD	Hard Disk Drive
I <sup>2</sup> C	Inter-Integrated Circuit
IP	Internet Protocol
LCD	Liquid Crystal Display
LEMT	LiPPERT Enhanced Management Technology
LED	Light Emitting Diode
LPC	Low Pin Count
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MMU	Memory Management Unit
PCI	Peripheral Component Interconnect
PHY	Physical Interface
PLL	Phase-Locked Loop
PWR	Power
SMB	System Management Bus
SMC	System Management Controller
SPI	Serial Peripheral Interface
SSD	Solid State Drive
SVGA	Super Video Graphics Array
TCP	Transmission Control Protocol
TLB	Translation Look-aside Buffer
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UDMA	Ultra-Direct Memory Access
UDP	User Datagram Protocol
VGA	Video Graphics Array
WDOG	Watchdog

# 1. Overview

## 1.1 Introduction

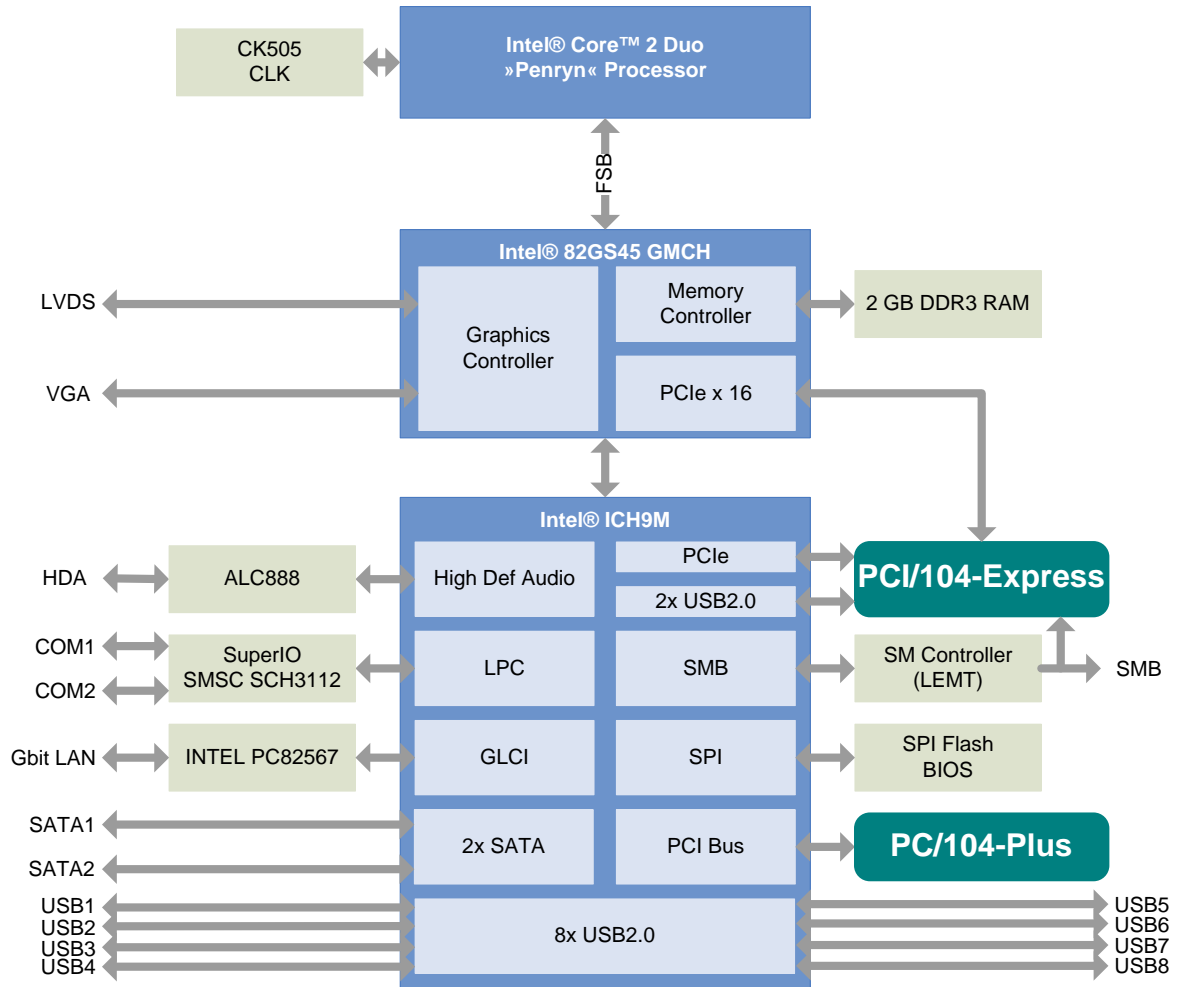
The PCI/104-Express board Cool XpressRunner-GS45 is designed for applications where a high performance x86 compatible, dual core processor boards is necessary. The board concept offers many standard I/O interfaces.

The Cool XpressRunner-GS45 is designed by using latest chipset technology platform from Intel, called Montevina. The CPU/chipset is on Intel's embedded roadmap, ensuring long time availability.

### *Features*

- Intel Core 2 Duo with Montevina chipset (SFF)
- Integrated graphics controller
- VGA, 1600 x 1200 pixels
- LVDS, 24/18 bits, 1600 x 1200 pixels
- Gigabit LAN
- 8 x USB 2.0
- 2 x SATA
- 2 x RS232/RS485
- 1 x 32-bit PC/104-Plus Slot
- 1 x PC104-Express Slot
- LEMT management functions
- Low power consumption
- Optionally extended temperature range -40 ... +85°C

**Block Diagram**



## 1.2 Ordering Information

### *Cool XpressRunner-GS45 Models*

Order number	Description
712-0001-10	CXR-GS45 PC/104-Express CPU board with ULV Intel Celeron M 722 processor (1.2GHz/800MHz FSB/1MB L2 cache), 1GB DDR3 RAM onboard. Operating temp. range: -0°C ... +60°C
712-0004-10	CXR-GS45 PC/104-Express CPU board with SP9300 Intel Core 2 processor (2.26GHz/1066MHz FSB/6MB L2 cache), 1 GB DDR3 RAM onboard. Operating temp. range: -0°C ... +60°C
712-0005-10	CXR-GS45 PC/104-Express CPU board with ULV Intel Celeron M 722 processor (1.2GHz/800MHz FSB/1MB L2 cache), 2GB DDR3 RAM onboard. Operating temp. range: -0°C ... +60°C
712-0006-10	CXR-GS45 PC/104-Express CPU board with SP9300 Intel Core 2 processor (2.26GHz/1066MHz FSB/6MB L2 cache), 2 GB DDR3 RAM onboard. Operating temp. range: -0°C ... +60°C
812-0001-10	CXR-GS45 PC/104-Express CPU board with ULV Intel Celeron M 722 processor (1.2GHz/800MHz FSB/1MB L2 cache), 1GB DDR3 RAM onboard. Operating temp. range: -20°C ... +60°C
812-0004-10	CXR-GS45 PC/104-Express CPU board with SP9300 Intel Core 2 processor (2.26GHz/1066MHz FSB/6MB L2 cache), 1 GB DDR3 RAM onboard. Operating temp. range: -20°C ... +60°C
812-0005-10	CXR-GS45 PC/104-Express CPU board with ULV Intel Celeron M 722 processor (1.2GHz/800MHz FSB/1MB L2 cache), 2GB DDR3 RAM onboard. Operating temp. range: -20°C ... +60°C
812-0006-10	CXR-GS45 PC/104-Express CPU board with SP9300 Intel Core 2 processor (2.26GHz/1066MHz FSB/6MB L2 cache), 2 GB DDR3 RAM onboard. Operating temp. range: -20°C ... +60°C
912-0001-10	CXR-GS45 PC/104-Express CPU board with Celeron 722 processor (1.2GHz/800MHz FSB/6MB L2 cache), 1 GB DDR3 RAM onboard. Operating temp. range: -40°C ... +85°C
912-0005-10	CXR-GS45 PC/104-Express CPU board with SP9300 Intel Core 2 processor (2.26GHz/1066MHz FSB/6MB L2 cache), 2 GB DDR3 RAM onboard. Operating temp. range: -40°C ... +60°C



**Note** Custom combinations of processor and memory are possible.  
Minimum order quantities are required.  
Contact LiPPERT's Sales Team at [sales@lippertembedded.com](mailto:sales@lippertembedded.com)

### *Cable Sets and Accessories*

Order number	Description
763-0018-10	Adapter Cable Set Power, GBit-Ethernet, VGA-CRT, 4x USB, COM1, COM2, 2x SATA, HD-Audio

## 1.3 Specifications

### *Electrical Specifications*

Supply voltage	+5 V DC
Rise time	< 10 ms
Supply voltage tolerance	± 5% *
Inrush current	5 A
Supply current	maximal 6.5 A depending on operating system and connected peripherals ** typical 2 A (Windows XP idle mode) typical 0.2 A (suspend to ram mode)

\* It is not guaranteed that all connected peripherals will work with that tolerance.

\*\* Measured with monitor, mouse, and keyboard only.  
Additional peripheral devices will increase the current.

### *Environmental Specifications*

#### *Operating:*

Temperature range	0 ... 60 °C (standard version, models with part numbers 7xx-xxxx-xx) -20 ... 60 °C (industrial version, models with part numbers 8xx-xxxx-xx) -40 ... 85 °C (extended version, models with part numbers 9xx-xxxx-xx)
Temperature change	max. 10K / 30 minutes
Humidity (relative)	10 ... 90 % (non-condensing)
Pressure	450 ... 1100 hPa

#### *Non-Operating/Storage/Transport:*

Temperature range	-40 ... 85 °C
Temperature change	max. 10K / 30 minutes
Humidity (relative)	5 ... 95 % (non-condensing)
Pressure	450 ... 1100 hPa

### *Mean Time Between Failures*

MTBF at 25°C	166504 hours
--------------	--------------

## 1.4 Mechanical

Dimensions (L x W)	115.6 mm x 95.9 mm (including I/O extension)
Height	max. 14 mm on top side above PCB max. 12 mm on bottom side above PCB
Weight	110 g
Mounting	4 mounting holes



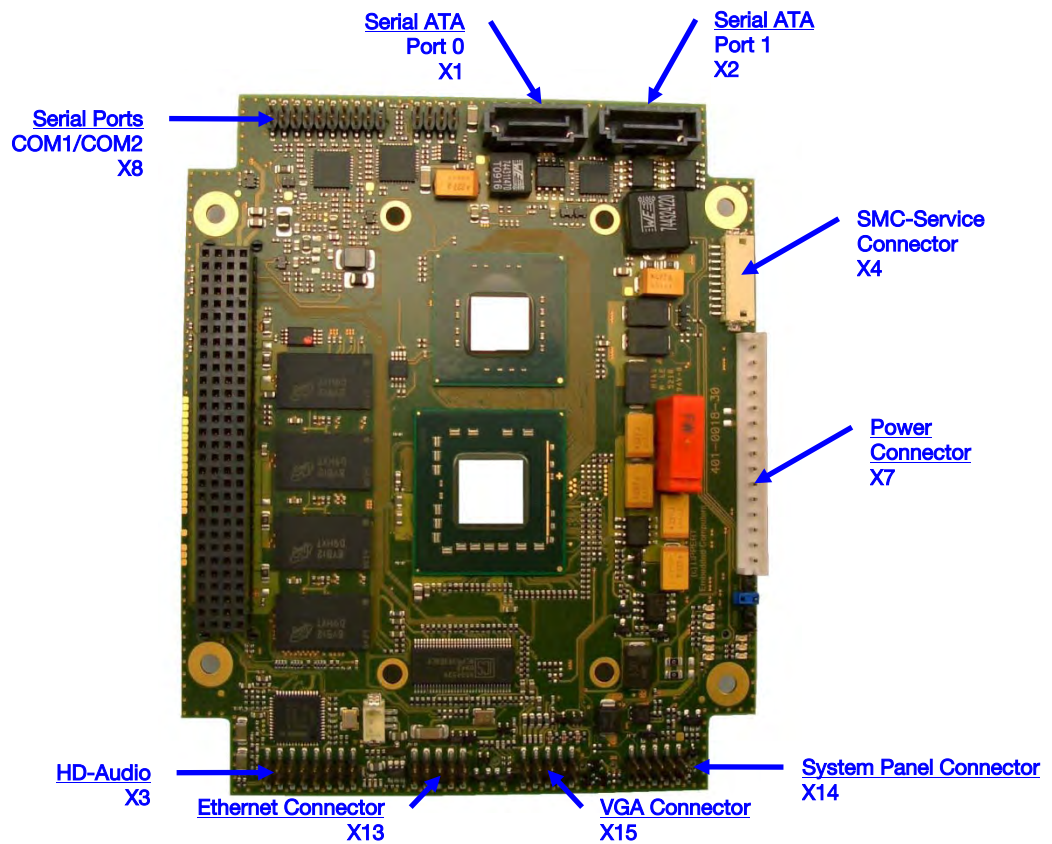
**Note** *It is strongly recommend using plastic spacers instead of metal spacers to mount the board. With metal spacers, there is a possible danger to create a short circuit with the components located around the mounting holes.  
This can damage the board!*

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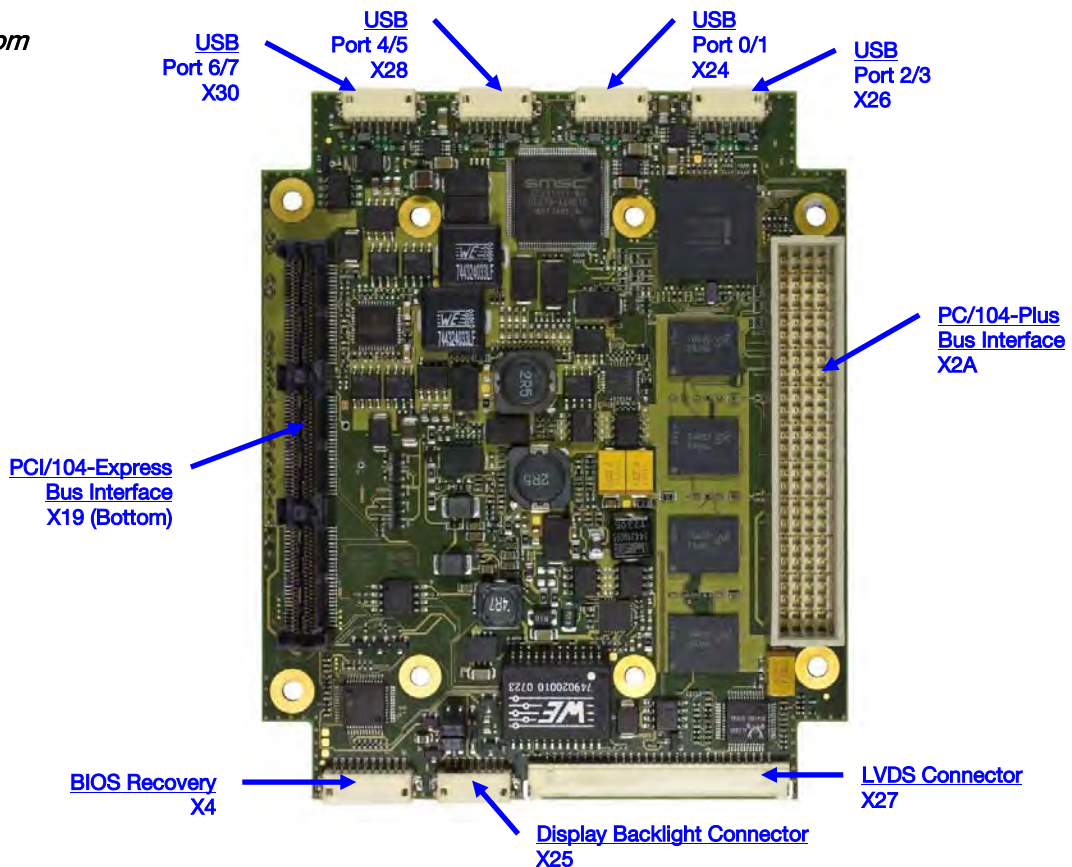
## 2. Getting Started

### 2.1 Connector Locations

*Top*

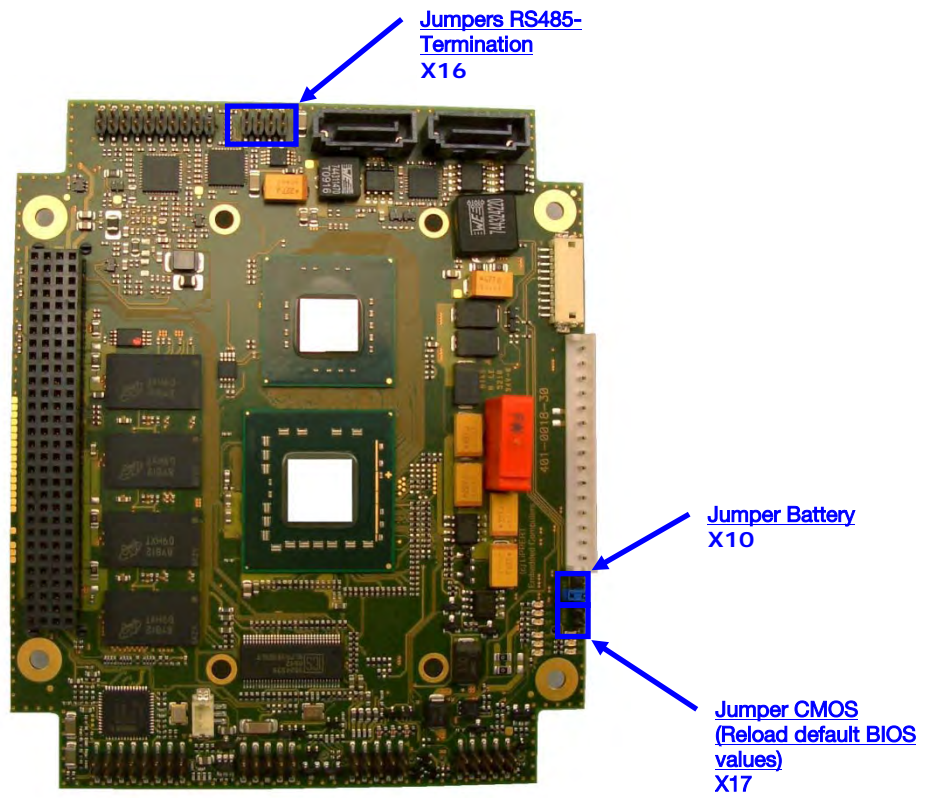


*Bottom*

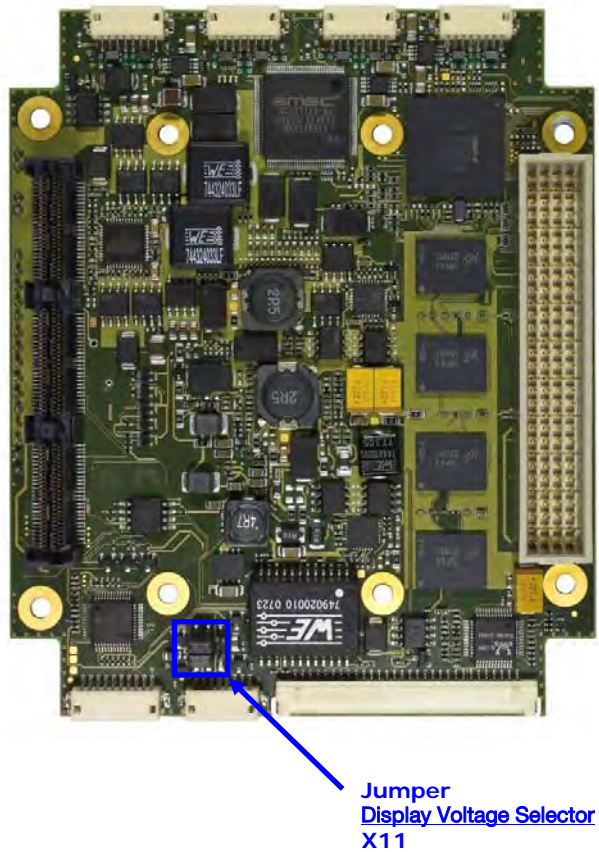


## 2.2 Jumper Locations

*Top*



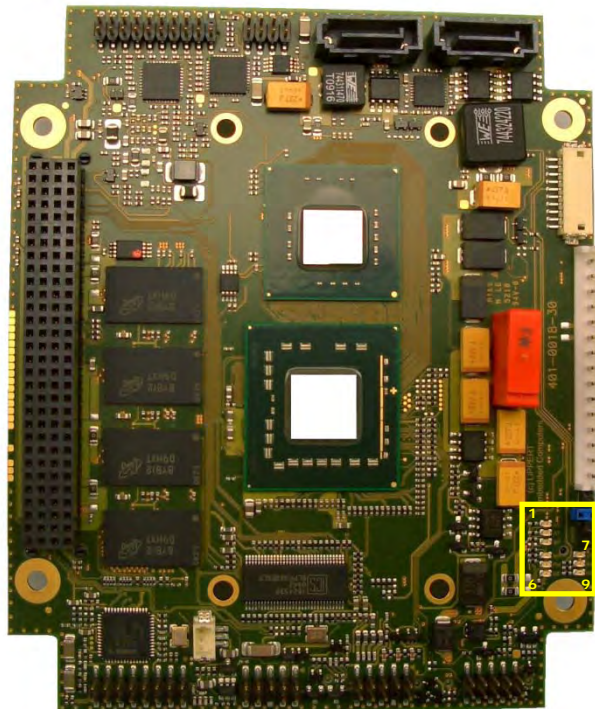
*Bottom*



## 2.3 LED Indicators

To facilitate problem solving, the Cool XpressRunner-GS45 provides LED indicators for the following conditions:

LED	Name	Function
1	LK	Ethernet link status
2	AT	Ethernet port activity
3	SP	Ethernet 1Gbit transfer rate
4	MP	Main Power Supply
5	PM	Power Mode
6	SB	Standby Power Supply
7	LV	Live Signal, indicates that the board's boot process was started
8	SA	Harddisk: SATA accesses
9	WD	Watchdog activated



## 2.4 Hardware Setup

Installing the Cool XpressRunner-GS45 is very straightforward. First, unpack the board observing the usual electrostatic discharge (ESD) precautions.

---



### **Caution**

Before you touch the board, make sure that you have discharged yourself and your gear towards a grounded terminal. Damages due to ESD are usually not immediately visible and will only show up later as failures in the field.

---

Mount the cooling device.

---



### **Caution**

Never operate the Cool XpressRunner-GS45 without suitable cooling devices. Failing this can destroy the module.

---



### **Caution**

Never connect or disconnect peripherals like hard drives while the board's power supply is connected and switched on!

---

Use the cable set provided by LiPPERT to connect the Cool XpressRunner-GS45 to a VGA monitor. Connect USB keyboard and mouse, respectively. Connect a hard drive with a SATA cable (not part of the cable set) to start an operation system. Make sure the pins match their counterparts correctly and are not bent! If you plan to use additional other peripherals, now is the time to connect them, too.

Connect a standard ATX with the adapter cable (art. no 862-0044-10) or a 5 volt, 8 amps power supply to the power connector and switch the power on.

---



**Note** *The 8 amps value is the minimum you should have for the standard peripherals mentioned. If you want to use more and/or others, please plan your power budget first! The system will not work if there is not enough supply current for all your devices.*

---

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS menu. See BIOS chapter for more details.

To load the BIOS default values plug in the jumper "CMOS" during startup. This forces the BIOS to load the factory settings from Flash.

The Cool XpressRunner-GS45 can boot from CD drives, USB floppy, USB stick, harddisk, or network. Provided any of these is connected and it contains a valid operating system image, the display then shows the boot screen of your operating system.

---



**Note** *Not all USB devices are suitable to boot the Cool XpressRunner-GS45. If there are problems, please try to use another device from another manufacturer.*

---

## 3. Module Description

### 3.1 Processor

Intel® Core™ 2 Duo Processor, 1.2 GHz ... 2.26 GHz.

The Penryn processor kernel on 45-nanometer process technology is a next generation high-performance, low-power mobile processor based on the Intel® Core™ micro architecture.

In the platform, the Penryn processor supports the Cantiga chipset and Intel® ICH9M I/O controller. This document contains electrical, mechanical and thermal specifications for:

- Dual Core Extreme edition (DC-XE)
- Standard voltage (SV)
- Low voltage (LV)
- Ultra-low voltage (ULV)

In this document, the Penryn processor is referred to as the processor and the Cantiga chipset is referred to as the (G)MCH. The following list provides some of the key features on this processor:

- Supports L1 cache-to-cache (C2C) transfer
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache in each core
- The Penryn processor in DC-XE, SV and LV have an On-die, up to 6-MB second level shared cache with Advanced Transfer Cache architecture
- The Penryn processor in ULV have an On-die, up to 3-MB second-level shared cache with Advanced Transfer Cache architecture
- Streaming SIMD extensions 2 (SSE2), streaming SIMD extensions 3 (SSE3), supplemental streaming SIMD extensions 3 (SSSE3) and SSE4.1 instruction sets
- The Penryn processor in DC-XE, SV and LV are offered at 1066-MHz source synchronous front side bus (FSB)
- The Penryn processor in ULV are offered at 800-MHz source-synchronous front side bus (FSB)
- Advanced power management features including Enhanced Intel Speed Step® Technology and dynamic FSB frequency switching
- Digital thermal sensor (DTS)
- Intel® 64 architecture
- Intel® Dynamic Acceleration Technology and Enhanced Multi Threaded Thermal Management (EMTTM)
- Supports PSI2 functionality
- The Penryn processor in SV is offered in Micro-FCPGA and Micro-FCBGA packaging technologies
- The Penryn SFF processor in LV and ULV are offered in Micro-FCBGA packaging technologies only
- Execute Disable Bit support for enhanced security
- C6 Low Power Feature with P\_LVL6 I/O Support

### 3.2 Northbridge

Intel® Cantiga (GS45) with Chipset Graphics and Memory Controller Hub (GMCH)

The (G)MCH manages the flow of information between various components through four main interfaces:

- Front Side Bus (FSB)
- System Memory Interface (DDR2)
- Graphics Interfaces (CRT, TV-Out, LVDS, SDVO, Display Port, iHDMI\* (DVI also) and PCI Express Graphics)
- Direct Management Interface (DMI)

For detailed information, please refer to the Intel® Cantiga datasheet.

### 3.3 Southbridge

The ICH9 provides extensive I/O support. Functions and capabilities include:

- *PCI Express Base Specification*, Revision 1.1 support
- *PCI Local Bus Specification*, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 3.0b
- Integrated Serial ATA host controllers with independent DMA operation on up to four ports and AHCI support.
- USB host interface with support for up to twelve USB ports; six UHCI host controllers; two EHCI high-speed USB 2.0 Host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- *System Management Bus (SMBus) Specification*, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Matrix Storage Technology (Intel® ICH9R, ICH9DH, ICH9DO, ICH9M, and ICH9M-E only)
- Supports Intel® Active Management Technology (Digital Office only)
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

### 3.4 Graphics Controller

This chapter details the chipset integrated graphics engines (3D, 2D and Video), 3D pipeline and their respective capabilities.

The (G)MCH graphics is powered by the Gen 5.0 Graphics Architecture and supports ten fully programmable execution cores, enabling greater performance than previous generation chipsets. Mobile Intel® 45 Express graphics supports full precision, floating-point operations to enhance the visual experience of compute-intensive applications.

The (G)MCH internal graphics devices (IGD) contain several types of components. The major components in the IGD are the engines, planes, pipes and ports. The (G)MCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines respectively. The IGD's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to memory, which are then retrieved and processed by (G)MCH planes.

#### ***VGA Connector (X15)***

Connector type: IDC10 pin header 2.00 mm  
Matching connector: IDC10 pin female connector 2.00 mm

Pin	Signal	Pin	Signal
1	Red	2	GND
3	Green	4	n.c.
5	Blue	6	CRT_DDC_CLK
7	HSYNC	8	CRT_DDC_DATA
9	VSYNC	10	GND



## LVDS

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics.

Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, each carry a portion of the data, thus doubling the throughput to a maximum theoretical pixel rate of 224 MP/s.

There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals.

There is a connector supplying the LC-Display's inverter.

### LVDS Connector (X27)

Connector type: Hirose DF14 30 pin header 1.25 mm, single row  
Matching connector: Hirose DF14-30S-1.25C, Part number 538-0012-3 00

Pin	Signal
1	VDD (3.3 V, opt.5 V)
2	VDD (3.3 V, opt.5 V)
3	GND
4	GND
5	TXA3 -
6	TXA3 +
7	TXACLK -
8	TXACLK +
9	GND
10	TXA2 -
11	TXA2 +
12	TXA1 -
13	TXA1 +
14	TXA0 -
15	TXA0 +
16	GND
17	TXB3 -
18	TXB3 +
19	TXBCLK -
20	TXBCLK +
21	GND
22	TXB2 -
23	TXB2 +
24	TXB1 -
25	TXB1 +
26	TXB0 -
27	TXB0 +
28	GND
29	LVDS DDC-CLK
30	LVDS DDC-DATA



"A" and "B" in the signal names denote the two possible LVDS channels.



### Caution

The maximum current on all supply pins is 1A!

### LVDS Color Mapping

	1	2	3	4	5	6	7
<b>CLKA</b>	1	1	0	0	0	1	1
<b>A0</b>	G2	R7	R6	R5	R4	R3	R2
<b>A1</b>	B3	B2	G7	G6	G5	G4	G3
<b>A2</b>	DE	VS	HS	B7	B6	B5	B4
<b>A3</b>	0/B1	B1	B0	G1	G0	R1	R0
<b>CLKB</b>	1	1	0	0	0	1	1
<b>B0</b>	G2	R7	R6	R5	R4	R3	R2
<b>B1</b>	B3	B2	G7	G6	G5	G4	G3
<b>B2</b>	DE	VS	HS	B7	B6	B5	B4
<b>B3</b>	0/B1	B1	B0	G1	G0	R1	R0

### Display Backlight Connector (X25)

Connector type: Hirose DF13 8 pin header 1.25 mm  
Matching connector: Hirose DF13-8S-1.25C, part number 536-0007-0 00

Pin	Direction	Signal
1	Output	+12 V DC, max. 1A
2	Output	+12 V DC, max. 1A
3	Output	+5 V DC, max. 1A
4	Output	+5 V DC, max. 1A
5	Output	Signal: Backlight Brightness Control (level: 3.3 V)
6	Output	Switched Inverter Power, max. 1A (refer to “Display Voltage Selector” below)
7		GND
8		GND



### Display Voltage Selector (X11)

Jumper for voltage selection of LVDS panels and backlight.

Connector type: IDC6 pin header 2.0 mm  
Matching part: 2.0 mm jumper

Use a 2mm jumper between 1-3 or 3-5 to select the backlight voltage.

Use a 2mm jumper between 2-4 or 4-6 to select the display voltage.

Pin	Signal	Pin	Signal
1	+3,3V DC	2	+12V DC
3	Display voltage	4	Backlight voltage
5	+5V DC	6	+5V DC



**Default jumper setting** is 3,3V for LVDS display and 12V for the inverter.



**Note** An arrow on the PCB marks Pin 1

### 3.5 Gigabit Ethernet Controller

Intel 82567 Physical Layer Transceiver (PHY)

The 82567 is a single port Gigabit Ethernet Physical Layer Transceiver (PHY) that connects to its MAC through a dedicated interconnect. The PHY is based on Intel's Gigabit PHY technology and supports operation at 1000/100/10 Mb/s data rates. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab).

The 82567 operates with the ICH9 chipset that incorporates the GbE MAC.

The PHY interfaces with its MAC through two interfaces: GLCI and LCI. GLCI is a high-speed serial interface based on 802.3 SerDes. LCI is a lower speed interface based on the 82562ET LCI interface. The PHY operates in a dual interface mode using GLCI for 1000 Mb/s traffic and LCI for all other traffic types.

*Ethernet Connector (X13)*

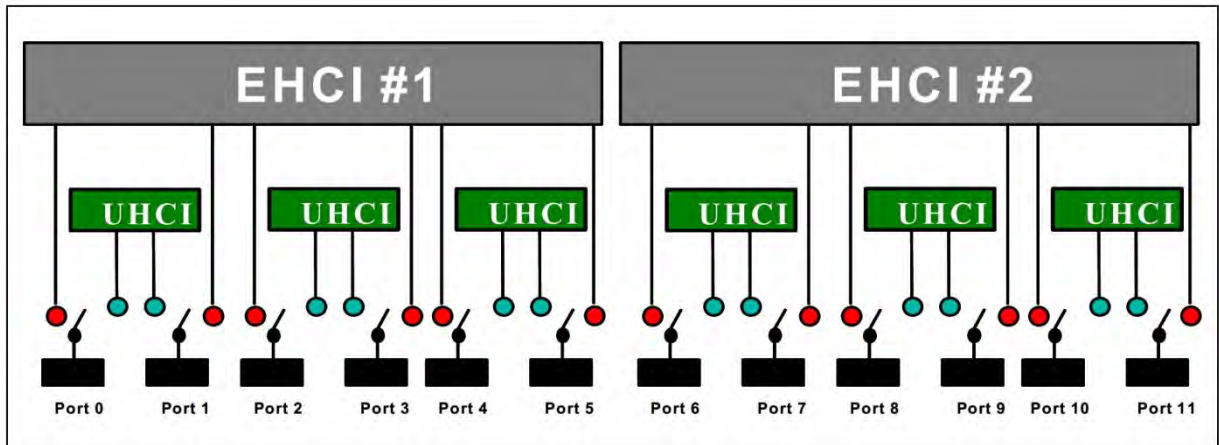
Connector type: IDC10 pin header 2.00 mm  
Matching connector: IDC10 pin female connector 2.00 mm

PIN	Signal	PIN	Signal
1	MX1-	2	MX1+
3	MX2-	4	MX2+
5	n.c.	6	n.c.
7	MX3-	8	MX3+
9	MX4-	10	MX4+



## 3.6 USB

The Southbridge (ICH9) contains two Enhanced Host Controller Interface (EHCI) host controllers, which support up to twelve USB 2.0 high-speed root ports. USB 2.0 allows data transfers up to 480Mb/s using the same pins as the twelve USB full-speed/low-speed ports. The ICH9 contains port-routing logic that determines whether a USB port is controlled by one of the UHCI controllers or by one of the EHCI controllers.



The Cool XpressRunner-GS45 uses ten of the twelve ports. Eight of the ten USB 2.0 host ports are available for the application on four USB connectors, each providing two ports. The ports 0 to 5 uses the first EHCI and the ports 6 to 7 use the second EHCI.

The other two USB 2.0 host ports are supported at the PCI/104-Express Bus Interface.

### ***USB Connectors (0-7; exemplary described USB 0/1; X24, X26, X28, X30)***

Connector type: Hirose DF13 8-pin header 1.25 mm  
Matching connector: Hirose DF13-8S-1.25C, part number 536-0007-0 00

PIN	Signal
1	VCC_USB0
2	USB0-
3	USB0+
4	USB-GND
5	USB-GND
6	USB1-
7	USB1+
8	VCC_USB1



### 3.7 Serial ATA

The ICH9 has two integrated SATA host controllers that support independent DMA operation on up to four ports and supports data transfer rates of up to 3.0Gb/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The ICH9 supports the Serial ATA Specification, Revision 1.0a. The Southbridge also supports several optional sections of the Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

The ICH9 provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (e.g., an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

There are two SATA ports available for the application on two SATA connectors.

#### ***SATA Connector (X1, X2)***

Connector type: SATA  
Matching connector: 7 pin Serial ATA plug

PIN	Signal
1	GND
2	Data_TX+
3	Data_TX-
4	GND
5	Data_RX-
6	Data_RX+
7	GND



### 3.8 HD-Audio

The ICH9's High Definition Audio (HDA) controller communicates with the external codec(s) over the Intel High Definition Audio serial link. The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The ICH9 implements four output DMA engines and four input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. ICH9 implements a single Serial Data Output signal (HDA\_SDOOUT) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The ICH9 implements four Serial Digital Input signals (HDA\_SDI[3:0]) supporting up to four codecs.

The Cool XpressRunner-GS45 uses a codec from Realtek. The ALC888 is a high-performance 7.1+2 Channel High Definition Audio Codec.

The following I/O's are used by the Cool XpressRunner-GS45:

- Analog Input (All ADC support 44,1k/48k/96kHz sampling rate)
  - Microphone left and right
  - Line In left and right
- Analog output (All DAC support 44,1k/48k/96/192kHz sampling rate)
  - Front left and right
  - Rear left and right
  - Center and Subwoofer
- Digital input (16/20/24-bit S/PDIF-in support 44,1k/48k/96/192kHz sampling rate)
  - S/PDIF
- Digital output (16/20/24-bit S/PDIF-out support 44,1k/48k/96/192kHz sampling rate)
  - S/PDIF

#### ***Audio Connector (X3)***

Connector type: IDC16 pin header 2.00 mm

Matching connector: IDC16 pin female connector 2.00 mm

Pin	Signal	Pin	Signal
1	Line-Out R	2	Line-Out L
3	Surrond R	4	Surrond L
5	LFE	6	Center
7	GND-Audio	8	GND-Audio
9	Line-In R	10	Line-In L
11	Mic R	12	Mic L
13	GND	14	GND
15	S/P-Dif IN	16	S/P-Dif OUT



### 3.9 BIOS Recovery

In order to recover from BIOS problems, a so-called recovery BIOS can be used. This is a special hardware unit that can be attached to the BIOS Recovery Connector.

#### *BIOS Recovery Connector (X4)*

Connector type: DF13 10 pin header 1.25 mm

Pin	Signal
1	+3V3
2	LPC_AD0
3	LPC_AD1
4	LPC_AD2
5	LPC_AD3
6	BIOS_DISABLE#
7	LPC_FRAME#
8	PCI_RST#
9	CLK_33_FWH_R
10	GND



#### **Caution**

The maximum current on the supply pin is 0.3A!

---

## 3.10 PCI/104-Express Bus Interface

The PCI Express architecture uses familiar software and configuration interfaces of the conventional PCI bus architecture, but provides a new high-performance physical interface while retaining software compatibility with the existing conventional PCI infrastructure.

PCI Express is a high performance I/O architecture used in both desktop and mobile applications. This hierarchical, point-to-point interconnect works well with on-board and slot oriented architectures. The purpose of this Specification is to adapt PCI Express to the stacked architecture employed with 104, EPIC and EBX form factor.

PCI/104-Express have the following features:

- Four x1 PCIe Lanes or one x4 PCIe Lane
- One x16 PCIe\* or optionally one x8 PCIe or one x4 PCIe or one x2 PCIe or two SDVO
- ATX power and control signals: +5V Standby, Power supply on, Power OK
- Power: +3.3V, +5V, +12V
- SMBus



**Note:** *The 3.3V pins on the PCI/104-Express bus are not supplied by the onboard 3.3V power supply by default (selectable via 0R0-Resistor-Jumpers). The maximum current is limited to 3.6 A. This Jumper position is for the supply via ATX (standard) or power supply module (via this Bus).*

*With 0R0-Resistor-Jumpers, the 3.3V pins can be supplied by the onboard 3.3V power supply, but with a lower current limit of 3 A. This Jumper position is for the supply with 5V only.*

*If a PCI/104-Express peripheral board needs 3.3V supply from the bus with more than these limits, then the peripheral must be supplied externally.*

---

\* x16 PCI Express port for external PCI Express-based graphics card.

## PCI/104-Express Connector (X19)

Connector type: Samtec ASP-129637-03  
 Matching connector: Samtec ASP-129646-03

PIN	Signal		PIN	Signal
1	GPIO0	+5V	2	PE_RST#
3	+3.3V		4	+3.3V
5	USB_1+		6	USB_0+
7	USB_1-		8	USB_0-
9	GND		10	GND
11	Pex1_1Tp		12	Pex1_0 Tp
13	Pex1_1Tn		14	Pex1_0 Tn
15	GND		16	GND
17	Pex1_2 Tp		18	Pex1_3 Tp
19	Pex1_2 Tn		20	Pex1_3 Tn
21	GND		22	GND
23	Pex1_1Rp		24	Pex1_0 Rp
25	Pex1_1Rn		26	Pex1_0 Rn
27	GND		28	GND
29	Pex1_2 Rp		30	Pex1_3 Rp
31	Pex1_2 Rn		32	Pex1_3 Rn
33	GND		34	GND
35	Pex1_1Clkp		36	Pex1_0Clkp
37	Pex1_1Clkn		38	Pex1_0Clkn
39	+5V_Always		40	+5V_Always
41	Pex1_2Clkp		42	Pex1_3Clkp
43	Pex1_2Clkn		44	Pex1_3Clkn
45	CPU_DIR		46	PWRGOOD
47	SMB_DAT		48	Pex16_Clkp
49	SMB_CLK		50	Pex16_Clkn
51	SMB_ALERT		52	PSON#



PIN	Signal		PIN	Signal
53	WAKE#	+5V	54	PEG_EN#
55	GND		56	GND
57	Pex16_0T(8)p		58	Pex16_0T(0)p
59	Pex16_0T(8)n		60	Pex16_0T(0)n
61	GND		62	GND
63	Pex16_0T(9)p		64	Pex16_0T(1)p
65	Pex16_0T(9)n		66	Pex16_0T(1)n
67	GND		68	GND
69	Pex16_0T(10)p		70	Pex16_0T(2)p
71	Pex16_0T(10)n		72	Pex16_0T(2)n
73	GND		74	GND
75	Pex16_0T(11)p		76	Pex16_0T(3)p
77	Pex16_0T(11)n		78	Pex16_0T(3)n
79	GND		80	GND
81	Pex16_0T(12)p		82	Pex16_0T(4)p
83	Pex16_0T(12)n		84	Pex16_0T(4)n
85	GND		86	GND
87	Pex16_0T(13)p		88	Pex16_0T(5)p
89	Pex16_0T(13)n		90	Pex16_0T(5)n
91	GND		92	GND
93	Pex16_0T(14)p		94	Pex16_0T(6)p
95	Pex16_0T(14)n		96	Pex16_0T(6)n
97	GND		98	GND
99	Pex16_0T(15)p		100	Pex16_0T(7)p
101	Pex16_0T(15)n		102	Pex16_0T(7)n
103	GND		104	GND

PIN	Signal		PIN	Signal
105	SDVO_DAT	+12V	106	SDVO_CLK
107	GND		108	GND
109	Pex16_OR(8)p		110	Pex16_OR(0)p
111	Pex16_OR(8)n		112	Pex16_OR(0)n
113	GND		114	GND
115	Pex16_OR(9)p		116	Pex16_OR(1)p
117	Pex16_OR(9)n		118	Pex16_OR(1)n
119	GND		120	GND
121	Pex16_OR(10)p		122	Pex16_OR(2)p
123	Pex16_OR(10)n		124	Pex16_OR(2)n
125	GND		126	GND
127	Pex16_OR(11)p		128	Pex16_OR(3)p
129	Pex16_OR(11)n		130	Pex16_OR(3)n
131	GND		132	GND
133	Pex16_OR(12)p		134	Pex16_OR(4)p
135	Pex16_OR(12)n		136	Pex16_OR(4)n
137	GND		138	GND
139	Pex16_OR(13)p		140	Pex16_OR(5)p
141	Pex16_OR(13)n		142	Pex16_OR(5)n
143	GND		144	GND
145	Pex16_OR(14)p		146	Pex16_OR(6)p
147	Pex16_OR(14)n		148	Pex16_OR(6)n
149	GND		150	GND
151	Pex16_OR(15)p		152	Pex16_OR(7)p
153	Pex16_OR(15)n		154	Pex16_OR(7)n
155	GND		156	GND



**Note:** The voltages +5V, +5VAlways and +12V are not generated by the onboard power-supply but routed from the Power Supply Connector. The maximum current limits are for each voltage:

+5V → 16.8A  
+5VAlways → 3.6A  
+12V → 8.4A

### 3.11 PC/104-Plus Bus Interface

The PC/104-Plus bus is a modification of the standard PCI bus. It allows all of the PC/104 features to be used, together with the high-speed PCI bus.

The main features are:

- PC/104-Plus Bus slot, fully compatible with PCI version 2.2 specifications.
- Integrated PCI arbitration interface (32 bit wide, 3.3V).
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 33 MHz PCI clock.
- Power: +3.3V, +5V, +12V, -12V



**Note:** *The 3.3V pins on the PC/104-Plus bus are not supplied by the onboard 3.3V power supply by default (selectable via OR0-Resistor-Jumpers). The maximum current is limited to 7.5 A. This Jumper position is for the supply via ATX (standard) or power supply module (via this Bus).*

*With OR0-Resistor-Jumpers the 3.3V pins can be supplied by the onboard 3.3V power supply, but with a lower current limit of 3.9 A. This Jumper position is for the supply with 5V only.*

*If a PC/104-Plus peripheral board needs 3.3V supply from the bus with more than that limit, it must be supplied externally.*

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## PC/104-Plus Connector (X2A)

Connector type: TEKA Interconnection Systems 2MR430-A7WN-368-0  
 Matching connector: TEKA Interconnection Systems 2MR430-A7WN-368-0 (bottom side)

Pin	A	B	C	D
1	GND	Reserved	+5 Volts	AD00
2	VI/O	AD02	AD01	+5 Volts
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	n.c.	C/BE1	AD15	n.c.
9	SERR	GND	SB0	PAR
10	GND	PERR	n.c.	SDONE
11	STOP	n.c.	LOCK	GND
12	n.c.	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	n.c.
14	GND	AD16	n.c.	C/BE2
15	AD18	n.c.	AD17	GND
16	AD21	AD20	GND	AD19
17	n.c.	AD23	AD22	n.c.
18	IDSELO	GND	IDSEL	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 Volts	AD28	AD27
22	+5 Volts	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	+5 Volts	GNT0
25	GNT1	VI/O	GNT2	GND
26	+5 Volts	CLK0	GND	CKL1
27	CLK2	+5 Volts	CLK3	GND
28	GND	INTD	+5 Volts	RST
29	+12 Volts	INTA	INTB	INTC
30	-12 Volts	REQ3	GNT3	GND



**Note:** All VI/O pins are connected to 5V in default, but it's also possible to connect VI/O via 0R0-Resistor-Jumper to 3.3V. The onboard power circuits supply them.  
 The voltages +5V, +12V and -12V are not generated by the onboard power-supply but routed from the Power Supply Connector. The maximum current limits are for each voltage:

+5V → 8A  
 +12V → 1A  
 -12V → 1A

### 3.12 Serial Ports

The maximum supported baud rates:

<u>RS485 mode</u>	1.5 Mbit/s
<u>RS232 mode</u>	430 Kbit/s

Two serial ports are located on one IDC header "COM". The ports either work in RS232 or RS485 mode, selectable in BIOS. When entering **Integrated Peripherals → SuperIO Device, Mode UART 1** and **Mode UART 2** can be selected. Termination resistors for RS485 Mode can be set with Jumpers on pin headers as described below.

To enable the transmitters of COM1 and COM2 in RS485 mode set the RTS# signal to '1'. Depending on your operating system driver's logic, this may mean setting a (non-inverted) RTS bit to '0' in your application software.

The serial ports are programmable in BIOS setup. When entering **Integrated Peripherals → SuperIO Device**, configuration of the serial ports is accessible.

The following settings are possible for COM1 and COM2:

- Disabled
- 3F8 / IRQ4 (base address / interrupt channel)
- 2F8 / IRQ3 (base address / interrupt channel)
- 3E8 / IRQ4 (base address / interrupt channel)
- 2E8 / IRQ3 (base address / interrupt channel)
- 4F8 / IRQ5 (base address / interrupt channel)
- 4E8 / IRQ7 (base address / interrupt channel)

The modes can be switched between RS232 and RS485.

#### **COM1/2 Connector (X8)**

Connector type: IDC20 pin header 2.00 mm  
Matching connector: IDC20 pin female connector 2.00 mm

Pin	RS232	RS485	Pin	RS232	RS485
1	DCD1	<i>Not used</i>	2	DSR1	RXD1+
3	RXD1	RXD1-	4	RTS1	TXD1+
5	TXD1	TXD1-	6	CTS1	<i>Not used</i>
7	DTR1	<i>Not used</i>	8	<i>Not used</i>	<i>Not used</i>
9	GND	GND	10	+5 Volts	+5 Volts
11	DCD2	<i>Not used</i>	12	DSR2	RXD2+
13	RXD2	RXD2-	14	RTS2	TXD2+
15	TXD2	TXD2-	16	CTS2	<i>Not used</i>
17	DTR2	<i>Not used</i>	18	<i>Not used</i>	<i>Not used</i>
19	GND	GND			



#### **Caution**

The maximum current on all supply pins is 0.5A!

### Jumpers RS485-Termination (X16)

Connector type: IDC8 pin header 2.00 mm  
 Matching part: 2.00 mm jumper

Use 2 mm jumpers to terminate lines correctly.

There are two jumpers COM1 and COM2, respectively.

The RS485 termination jumpers are located at the top of the printed circuit board, see chapter 2.2. **Default setting is all jumpers off.**

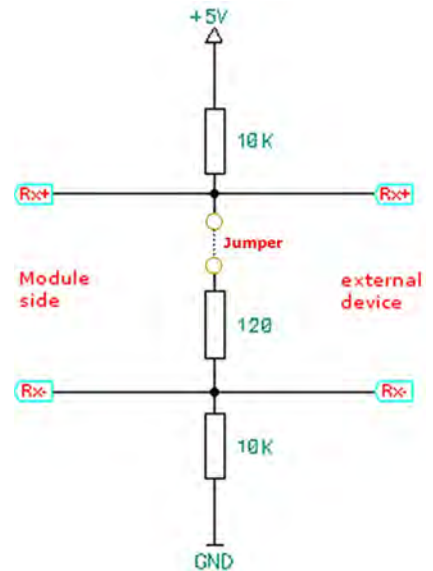
Pin	Signal	Pin	Signal
1	TX1+	2	TX1-
3	RX1+	4	RX1-
5	TX2+	6	TX2-
7	RX2+	8	RX2-



When the jumper is set, the differential pairs are terminated with 120Ω between them. (e.g. RX+ and RX-, on the right picture)

Additionally, positive/negative receive lines are pulled up/down with 10kΩ to 5V/GND in order to protect the transceivers of the Cool XpressRunner-GS45 from overvoltage.

It is recommended to protect the ports of the external device in the same way!



**Caution:** Termination resistors **should not** be used in RS232 Model! Otherwise, the serial ports will not work.

### 3.13 On Board Power Supply

The on board power supply generates all necessary voltages from the single supply voltage of 5 volts. The generated 3.3 volts are available on the connectors "System Panel" and "LVDS".



**Note** This 3.3 V must not be used to supply external electronic devices with high power consumption like other PC/104 boards or displays.

The 3.3V\* (also 5V, 12V, (-12V)) available on the PC104 Plus and PCI/104-Express Connectors is delivered directly from the external power supply unit, so refer to the specification of your power supply unit for information on maximum available power on the PC104 Plus and PCI/104-Express connectors.

ATX or single voltage (5V DC) supplies can be connected via an adapter cable.

#### Power Connector (X7)

Connector type: JST B15B-EH-A 15 pin  
 Matching connector: JST EHR-15 15 pin female connector

Pin	Signal (standard)	Signal (5V only)
1	+V5IN	+V5IN
2	GND	GND
3	+V5IN	+V5IN
4	GND	GND
5	+V5IN	+V5IN
6	+V5A	+V5A (or +V5IN)
7	GND	GND
8	PSON#	n.c.
9	PWROK	n.c.
10	+V3.3IN	n.c.
11	GND	GND
12	+12V (only for PCI slot and backlight power supply)	n.c.
13	+12V (only for PCI slot and backlight power supply)	n.c.
14	GND	GND
15	-12V (only for PCI slot)	n.c.



**Note** The default cable adapter supports the connection of  $\pm 12V$  power supply. If the 5V only power supply is required leave these pins open. The board can also be supplied over PCI/104-Express- or PC/104 plus bus. For this, connect the pins 5 and 6 (via 0R0-Resistor-Jumper beside Power Connector).

\* The 3.3V which is available on the PC104 Plus and PCI/104-Express Connectors can also delivered from the internal power supply of the Board via 0R0-Resistor-Jumper. But this option is only necessary if you power with 5V only and even need the 3.3V at the PC104 Plus and PCI/104-Express Connectors. Do not forget to change back the Jumpers if you change from 5V only to ATX (standard), because this can destroy the internal power supply.

#### Real Time Clock Backup

A battery is integrated on board. This battery is necessary to power the real-time clock (RTC) if the power supply is switched off. For this you have to connect the "BAT"-Jumper, which is not connected as default.

Battery Type: CR1225, 3 Volt

### 3.14 System Panel Connector

That connector is used by a different kind of signals. There is no standard cable adapter available.

#### System Panel Connector (X14)

Connector type: IDC10 pin header 2.00 mm  
 Matching connector: IDC10 pin female connector 2.00 mm



#### SMBus/I<sup>2</sup>C

The ICH9 contains a SMBus (System Management Bus) Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I<sup>2</sup>C devices. Special I<sup>2</sup>C commands are implemented.

The ICH9's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). In addition, the ICH9 supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface: Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

ICH9's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide addresses to all SMBus devices.

At these Pins are also the Ethernet LED's supported via 0R0-Resistor-Jumpers, but the default Jumper is for SMB.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

#### Power-Button

To power up/down the board the signal Power-Button must be pulled to GND. At the Pin Power Button is also the Ethernet LED Speed supported via 0R0-Resistor-Jumpers, but the default Jumper is for Power Button.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

#### Reset-Button

To reset the board, the signal Reset-Button must be pulled to GND.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

#### HDD-LED

To see the HDD activation external, the signal "HDD LED" must be pulled to +3.3V.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

## Watchdog

To see the Watchdog activation external, the signal "Watchdog" must be pulled to +3.3V.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

## External Battery

A connected external battery should replace or support the mounted one to keep date and time up to date. It is recommended to use a model with 3 Volt (Suggestion: CR2032). The time and date will be lost if the power supplier falls to 2.0 Volt.

For live time calculation there are 5  $\mu$ A (25°C) needed when the board is not running. That value can rise up depending on the connected cables and higher temperatures.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

## Ethernet LED's LK, AT and SP

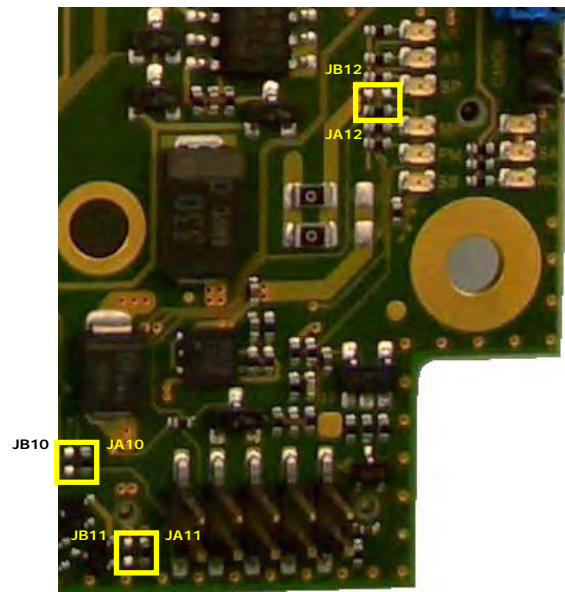
To see the Ethernet LED's Link, Activity and Speed external you have to change some 0R0-Resistor-Jumpers, because as default the Signals SMB\_CLK, SMB\_DATA and Power Button are at these Pins.

Pin	Signal	Pin	Signal
1	SMB_CLK / ETH LINK	2	SMB_DATA / ETH ACT
3	Power Button / ETH SPEED	4	Ext. Battery
5	GND	6	HDD LED
7	Reset Button	8	+3.3V
9	GND	10	Watchdog

The following picture shows the location of the 0R0-Resistor-Jumpers. The table describes the relation of Resistor-Jumpers and signals.

Resistor Jumper	Signal
JA10	SMB_CLK
JA11	SMB_DATA
JA12	Power Button
JB10	ETH LINK
JB11	ETH ACT
JB12	ETH SPEED

Default Resistor-Jumper settings.



### 3.15 Watchdog

A watchdog timer is integrated in the system management microcontroller and handled by the LEMT software. If a watchdog event occurred, the watchdog LED is lit after restart.

### 3.16 LEMT functions

The onboard Microcontroller implements power sequencing and LEMT (LiPPERT Enhanced Management Technology) functionality. The microcontroller communicates via the System Management Bus with the CPU/Chipset. The following functions are implemented:

- Total operating hours counter  
Counts the time the module has been run in minutes.
- On-time minutes counter  
Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature  
Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Watchdog Timer  
Set / Reset / Disable Watchdog Timer.
- System Restart Cause  
Power loss / Watchdog / External Reset.
- Fail-Safe-BIOS Support  
In case of a Boot failure, hardware signals tells external logic to boot from Fail-Safe-BIOS.
- Flash area  
1kB Flash area for customer data
- Protected Flash area  
128 Bytes for Keys, ID's, etc. can stored in a write- and clear-protectable region.
- Board Identify  
Vendor / Board / Serial number

The LEMT Tools are available for Windows and Linux. LEMT functionality can also be used in applications. Please ask our support for the LEMT software manual and technical manual regarding more details on its functionality and how to use it.

## Board Specific LEMT functions

### Voltages

The SMC of the CXR-GS45 implements a Voltage Monitor and samples several Onboard-Voltages. The Voltages can be read by calling the LEMT function "Get Voltages". The function returns a 16 Bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

ADC Channel	Voltage Name	Voltage Formula [V]
0	---	---
1	+V1.5S	$(MSB \ll 8 + LSB) * 3.3 / 1024$
2	+V3.3A	$(MSB \ll 8 + LSB) * 1.100 * 3.3 / 1024$
3	+V0.75	$(MSB \ll 8 + LSB) * 3.3 / 1024$
4	+V1.5	$(MSB \ll 8 + LSB) * 3.3 / 1024$
5	+V1.05M	$(MSB \ll 8 + LSB) * 3.3 / 1024$
6	+V1.8M_WOL	$(MSB \ll 8 + LSB) * 3.3 / 1024$
7	+V5A	$(MSB \ll 8 + LSB) * 1.833 * 3.3 / 1024$

### TS#-Events

TS# is activated by the Northbridge Temperature sensor when its critical temperature is reached and released when the device is back into its normal temperature range. This counter gives the User information of Temperature/Cooling problems. This counter is cleared when the system is removed from power.

### Exception Codes

In case of an error the SMC shows a blink code on the STATUS-LED. This error code is also reported by the SMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore the "Clear Exception Code"-Command is not supported.

Exception Code	Error Message
0	NO_ERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S3
5	RESET_FAIL
6	NO_PWRGD_3V3A
8	NO_PWRGD_ALL_SYS
11	+V1.5S
12	+V3.3A
13	+V0.75
14	+V1.5
15	+V1.05M
16	+V1.8M_WOL
17	+V5A
18	BIOS_FAIL
19	LOW_VIN

### **SMC Flags**

The SMC Flags return the last detected Exception Code since Power-up. The upper 3 bits of the SMC Flags register are reserved for future use.

### **SMC Status**

This register show of the status of SMC controlled signals on the CXR-GS45.

Status Bit	Signal
0	SMC_WDACTIVE#
1	-
2	-
3	-
4	-
5	-
6	-
7	-

## **3.17 CPU Fan Supply**

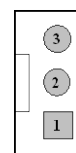
The Cool XpressRunner-GS45 provides a connector to power a CPU fan if the module is actively cooled.

### **CPU Fan Connector (X12)**

Connector type: Hirose DF13 3 pin header 1.25 mm

Matching connector: Hirose DF13-3S-1.25C, part number 536-0002-7 00

Pin	Signal
1	Speed Signal from fan (yellow)
2	+5VDC (red)
3	GND (black)



## 4. Using the Module

### 4.1 BIOS

The Cool XpressRunner-GS45 is delivered with a Phoenix –Award PC bios. The default setting guarantees a "ready to run" system, even without a BIOS setup backup battery.

All setup changes of the BIOS are stored in the CMOS RAM. A copy of the CMOS RAM, excluding date and time, is stored in the flash memory. This means that even if the backup battery runs out of power, the BIOS settings are not lost. Only date and time will be reset to their default value.

The soldered battery will keep that information over 2 years without any activation of the board. That depends on the use of the board. When power is up, the battery does not lose capacity.

The BIOS can be easily updated on board with software under DOS.

#### *Jumper BAT (Battery)*

Removal of the jumper "BAT" increases the lifetime of the battery. In that case the battery only loses capacity over self-discharge. If the jumper is not connected, then in the BIOS the settings will still keep their information, because of the flash storage. Except the Real Time Clock will not be up to date.

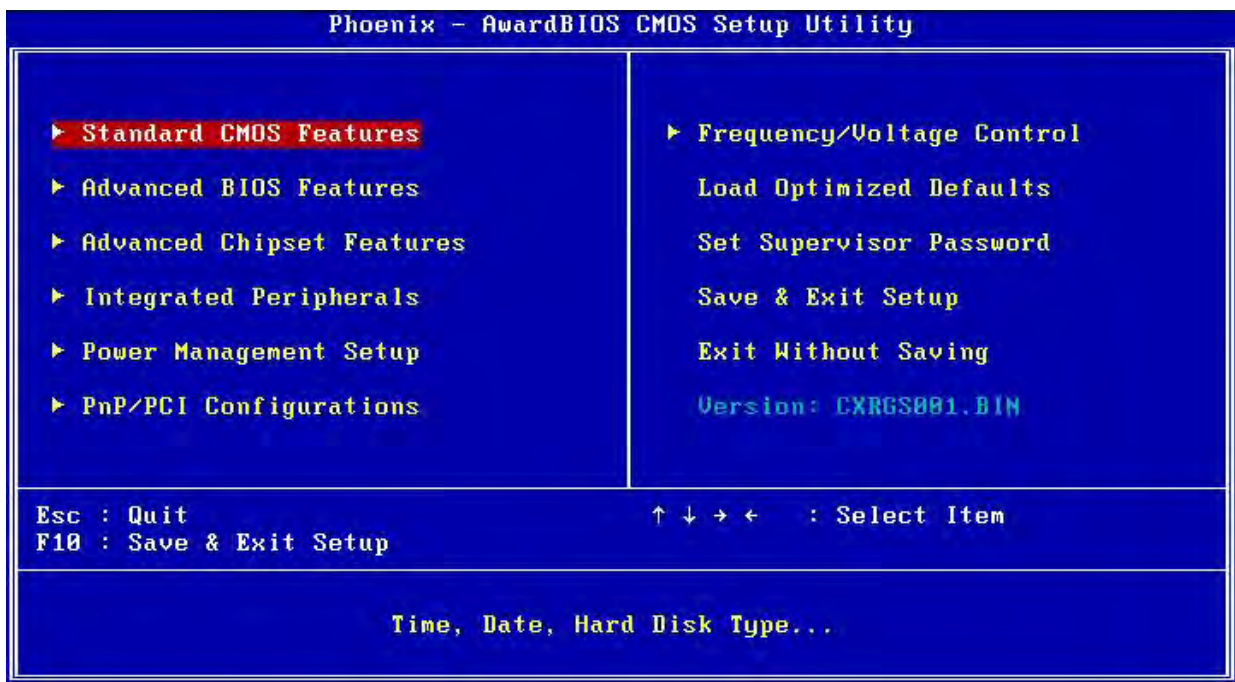
**As default, the jumper battery is not set.**



**Note** *It is recommended to set the jumper battery for proper operation before actually using the module.*

#### *Setup*

Pressing <DEL> at power-up starts the setup utility.



#### *Initialize BIOS at first startup*

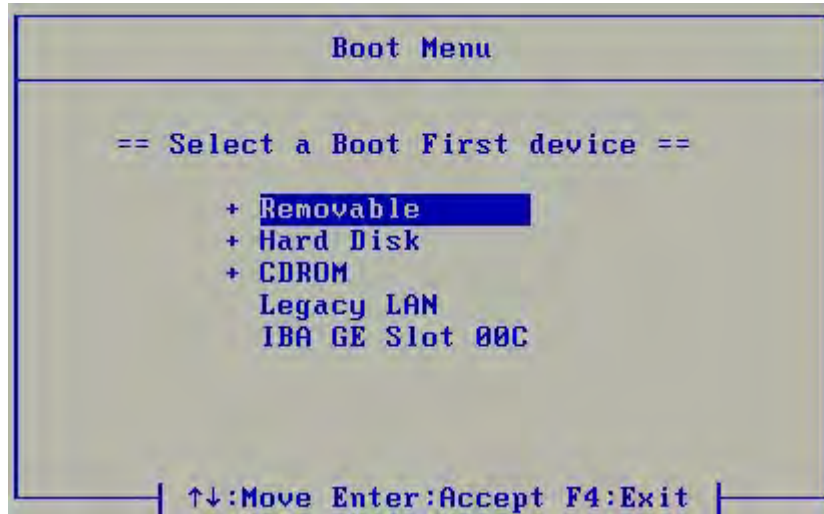
It is important to initialize the BIOS setting at first startup of the board.

Call setup by pressing <DEL> at power-up and executed **Load Optimized Defaults**. Then use **Save & Exit Setup** to save and activate the new settings.

The "Optimized Defaults" is the optimized BIOS setup for the Cool XpressRunner-GS45

### Booting from alternative device (Boot Menu)

Pressing the <ESC> key at power-up starts the Boot Menu. Choose one of the listed bootable devices for booting.



Without entering the BIOS Setup a boot device can be selected manually.



Connected Devices like USB hard drive or hard drive disks are listed in the Hard Disk menu.

### ***Jumper CMOS (Reload default BIOS values)***

In rare cases, it can happen that the system does not start because of certain BIOS settings. If that is the case, it is highly recommend to first restoring the BIOS factory settings before any debugging is done. This is achieved with **Load Optimized Defaults** in the main setup menu. If you cannot reach the BIOS setup because of bad system configuration, use the jumper **CMOS** near the power connector.

- Power off the board
- Set the 2.00 mm jumper **CMOS**
- Power on the board

**As default, the jumper CMOS is not set.**

You will see the following message:

A screenshot of a BIOS boot screen with a black background and white text. The text reads: "AHCI Option ROM BIOS Revision: 01.06.70 Date: 08-13-2008", "Copyright (c) 2006-2008 Phoenix Technologies, LTD", "AHCI BIOS not installed!!", and "Override enabled - Defaults loaded". A small dash is visible at the bottom left of the screen.

```
AHCI Option ROM BIOS Revision: 01.06.70 Date: 08-13-2008
Copyright (c) 2006-2008 Phoenix Technologies, LTD

AHCI BIOS not installed!!

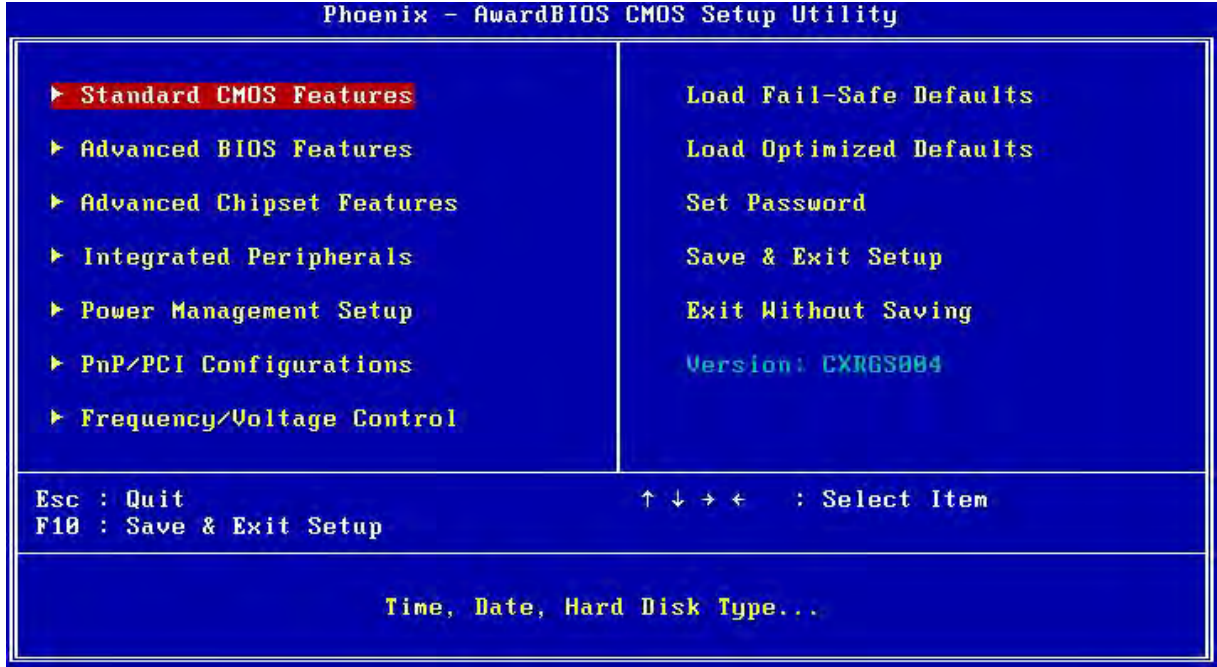
Override enabled - Defaults loaded
-
```

Then press **<DEL>** and use **Save & Exit Setup** to continue with default setup values and remove the jumper "CMOS".

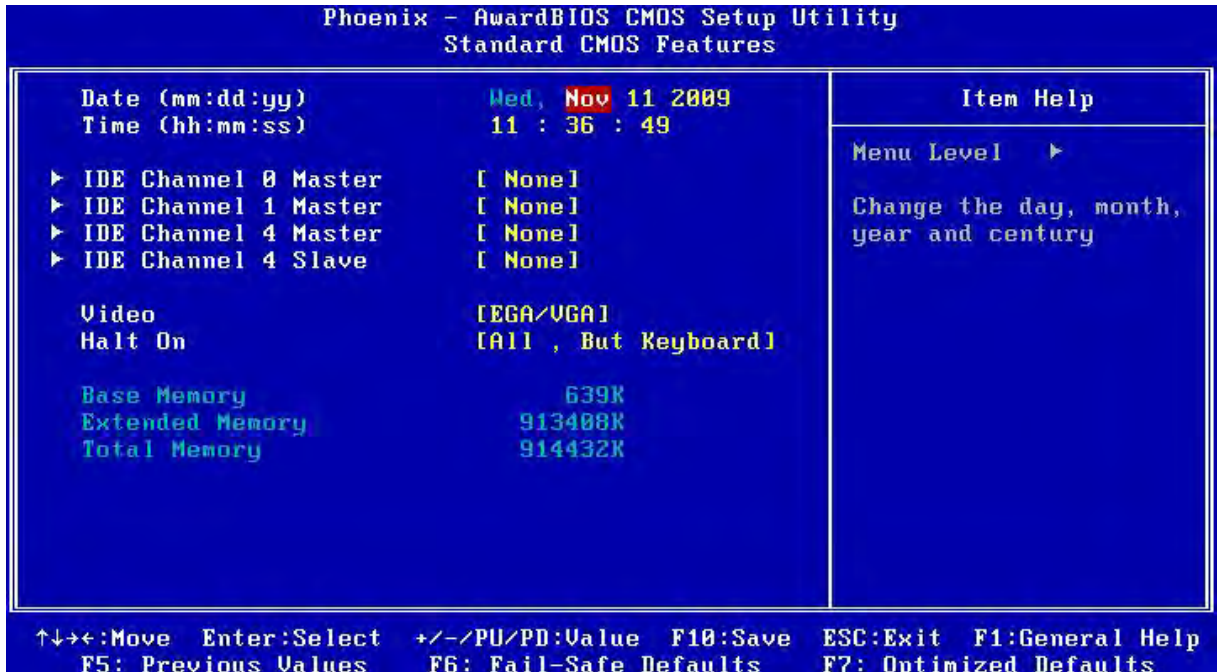
## BIOS Screens

The BIOS setup utility allows setting of various board parameters. The following pictures show the different setup menus. The Cool XpressRunner-GS45 specific settings are explained here.

### Phoenix – Award BIOS Start Screen



### Standard CMOS Features



*Advanced BIOS Features, part 1*

Phoenix - AwardBIOS CMOS Setup Utility  
Advanced BIOS Features

<ul style="list-style-type: none"> <li>▶ CPU Feature [Press Enter]</li> <li>▶ Hard Disk Boot Priority [Press Enter]</li> <li>Virus Warning [Disabled]</li> <li>Quick Power On Self Test [Enabled]</li> <li>First Boot Device [Hard Disk]</li> <li>Second Boot Device [CDROM]</li> <li>Third Boot Device [Legacy LAN]</li> <li>Boot Other Device [Enabled]</li> <li>Boot Up NumLock Status [On]</li> <li>Typematic Rate Setting [Disabled]</li> <li>× Typematic Rate (Chars/Sec) 6</li> <li>× Typematic Delay (Msec) 250</li> <li>Security Option [Setup]</li> <li>APIC Mode Enabled</li> <li>MPS Version Control For OS[1.4]</li> <li>OS Select For DRAM &gt; 64MB [Non-OS2]</li> <li>Console Redirection Disabled</li> <li>× Baud Rate 19200</li> <li>Agent after boot Enabled</li> </ul>	<p>Item Help</p> <hr/> <p>Menu Level ▶</p>
--	--

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Advanced BIOS Features, part 2*

Phoenix - AwardBIOS CMOS Setup Utility  
Advanced BIOS Features

<ul style="list-style-type: none"> <li>Typematic Rate Setting [Disabled]</li> <li>× Typematic Rate (Chars/Sec) 6</li> <li>× Typematic Delay (Msec) 250</li> <li>Security Option [Setup]</li> <li>APIC Mode [Enabled]</li> <li>MPS Version Control For OS[1.4]</li> <li>OS Select For DRAM &gt; 64MB [Non-OS2]</li> <li>Console Redirection Disabled</li> <li>× Baud Rate 19200</li> <li>Agent after boot Enabled</li> <li>Full Screen LOGO Show [Enabled]</li> <li>Summary Screen Show [Disabled]</li> <li>ASF support [Enabled]</li> <li>DMI Event Log [Enabled]</li> <li>Clear All DMI Event Log [No]</li> <li>View DMI Event Log [Enter]</li> <li>Mark DMI Events as Read [Enter]</li> <li>Event Log Capacity Space Available</li> <li>Event Log Validity Valid</li> </ul>	<p>Item Help</p> <hr/> <p>Menu Level ▶</p> <p>Description :</p> <p>Clear all DMI event logs immediately.</p> <p>Press [Enter] will pop up a confirm screen. Hit [Y] and [enter], then clear all DMI event logs right now.</p>
---	---

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Advanced BIOS Features – CPU Feature (Penryn)*

Phoenix – AwardBIOS CMOS Setup Utility		CPU Feature	
C1E Function	[Auto]	Item Help	
CPU C State Capability	[Disable]	Menu Level ▶	
Execute Disable Bit	[Enabled]	CPU C1E Function	
Virtualization Technology	[Disabled]	Select	
Core Multi-Processing	[Enabled]		

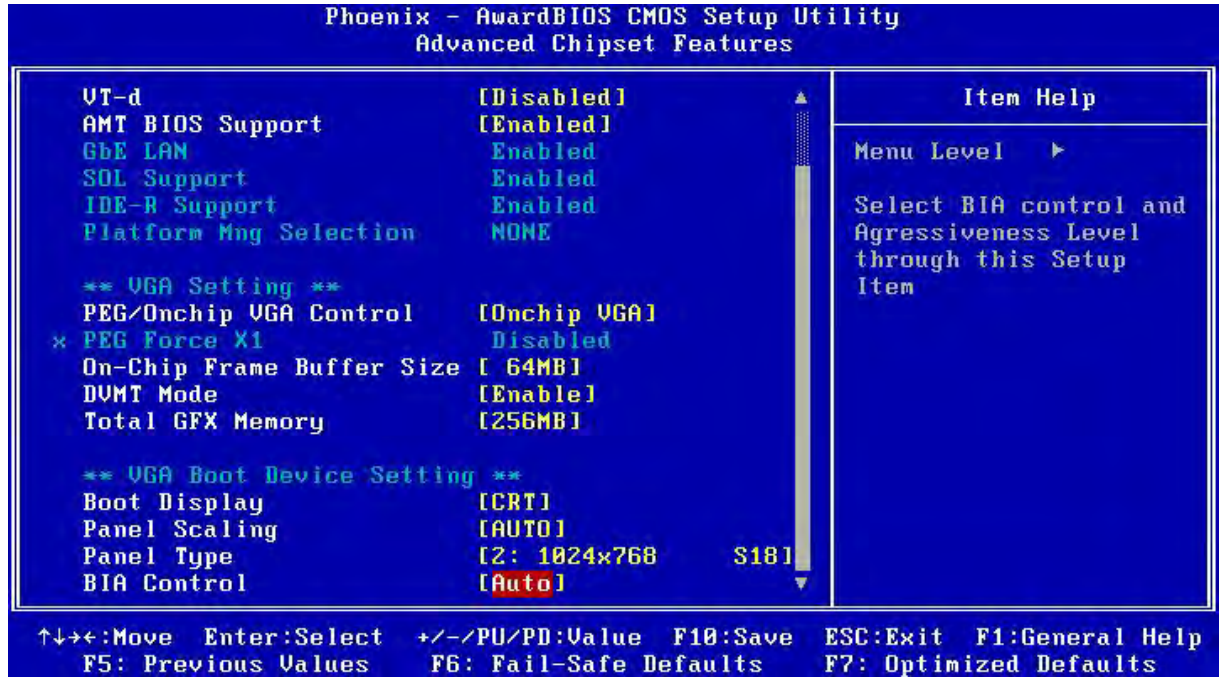
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Advanced BIOS Features – CPU Feature (Celeron M722)*

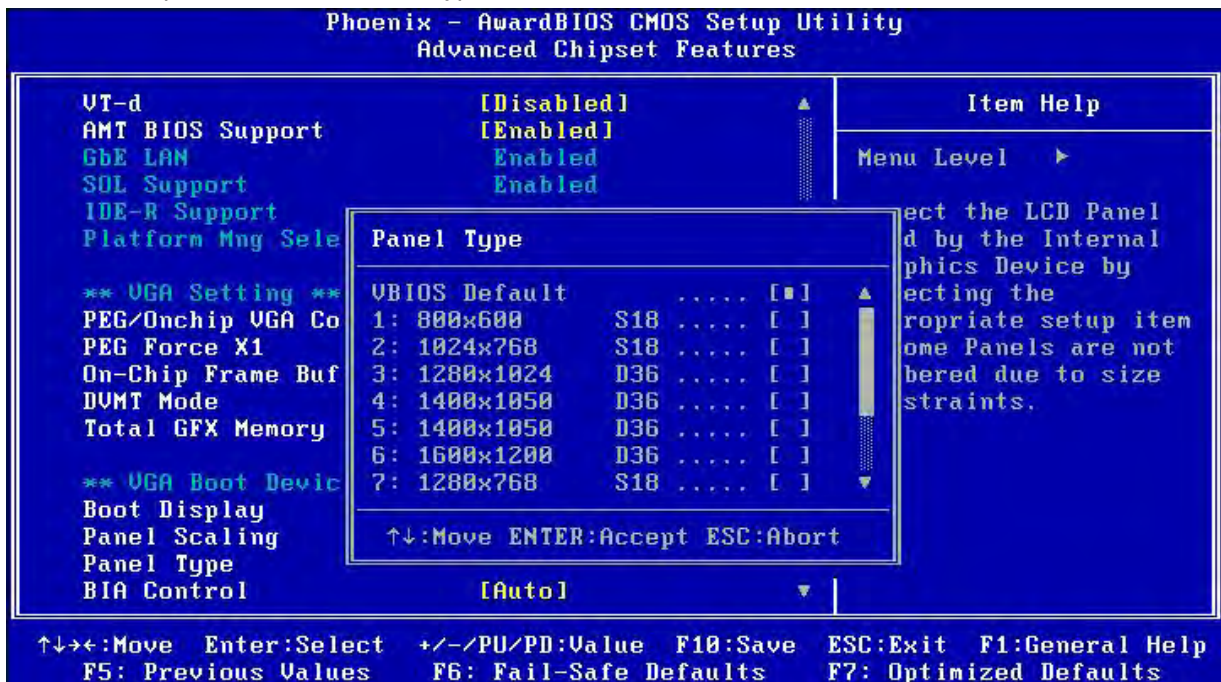
Phoenix – AwardBIOS CMOS Setup Utility		CPU Feature	
C1E Function	[Auto]	Item Help	
CPU C State Capability	[Disable]	Menu Level ▶	
Execute Disable Bit	[Enabled]	CPU C1E Function	
Core Multi-Processing	[Enabled]	Select	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Advanced Chipset Features*



*Advanced Chipset Features – Panel Type*



With the Panel Type settings, the display interface can be configured. States marked with "S" are for single channel, states marked with "D" for dual channel operation. The numbers give the screen resolution used for the display.

*Integrated Peripherals*

Phoenix - AwardBIOS CMOS Setup Utility		Item Help
Integrated Peripherals		Menu Level ▶
▶ OnChip IDE Device	[Press Enter]	
HOST Mac Address	00-00-00-00-00-00	
▶ SuperIO Device	[Press Enter]	
▶ USB Device Setting	[Press Enter]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Integrated Peripherals - OnChip IDE Device*

Phoenix - AwardBIOS CMOS Setup Utility		Item Help
OnChip IDE Device		Menu Level ▶
IDE HDD Block Mode	[Enabled]	
IDE DMA transfer access	[Enabled]	
IDE Primary Master PIO	[Auto]	
IDE Primary Master UDMA	[Auto]	
IDE Secondary Master PIO	[Auto]	
IDE Secondary Master UDMA	[Auto]	
SATA Mode	[IDE]	
LEGACY Mode Support	[Disabled]	
x Robson Support	Disabled	

If your IDE hard drive supports block mode select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Integrated Peripherals – SuperIO Device*

Phoenix – AwardBIOS CMOS Setup Utility		Item Help
SuperIO Device		Menu Level ▶
Onboard Serial Port 1	[3F8/IRQ4]	
Mode UART 1	[RS232]	
Onboard Serial Port 2	[2F8/IRQ3]	
Mode UART 2	[RS232]	

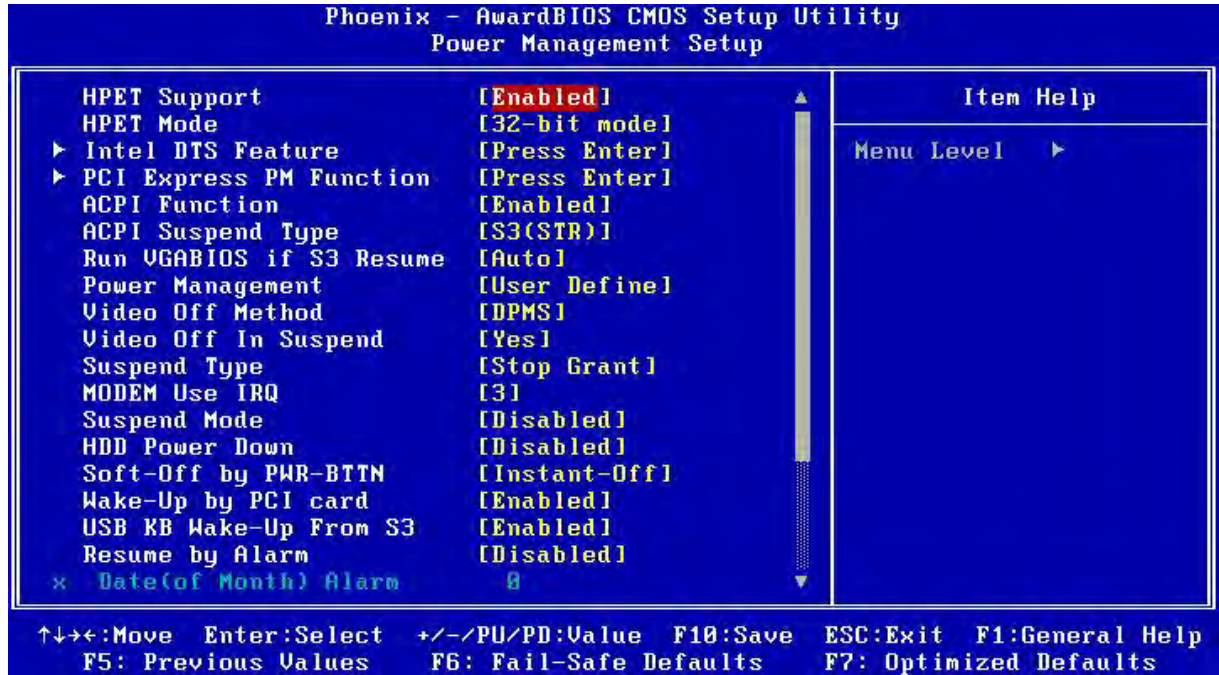
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

*Integrated Peripherals – USB Device Setting*

Phoenix – AwardBIOS CMOS Setup Utility		Item Help
USB Device Setting		Menu Level ▶
USB 1.0 Controller	[Enabled]	
USB 2.0 Controller	[Enabled]	
USB Operation Mode	[High Speed]	
USB Keyboard Function	[Enabled]	
USB Mouse Function	[Enabled]	
USB Storage Function	[Enabled]	
*** USB Mass Storage Device Boot Setting ***		[Enabled] or [Disable] Universal Host Controller Interface for Universal Serial Bus.

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

Power Management Setup, part 1



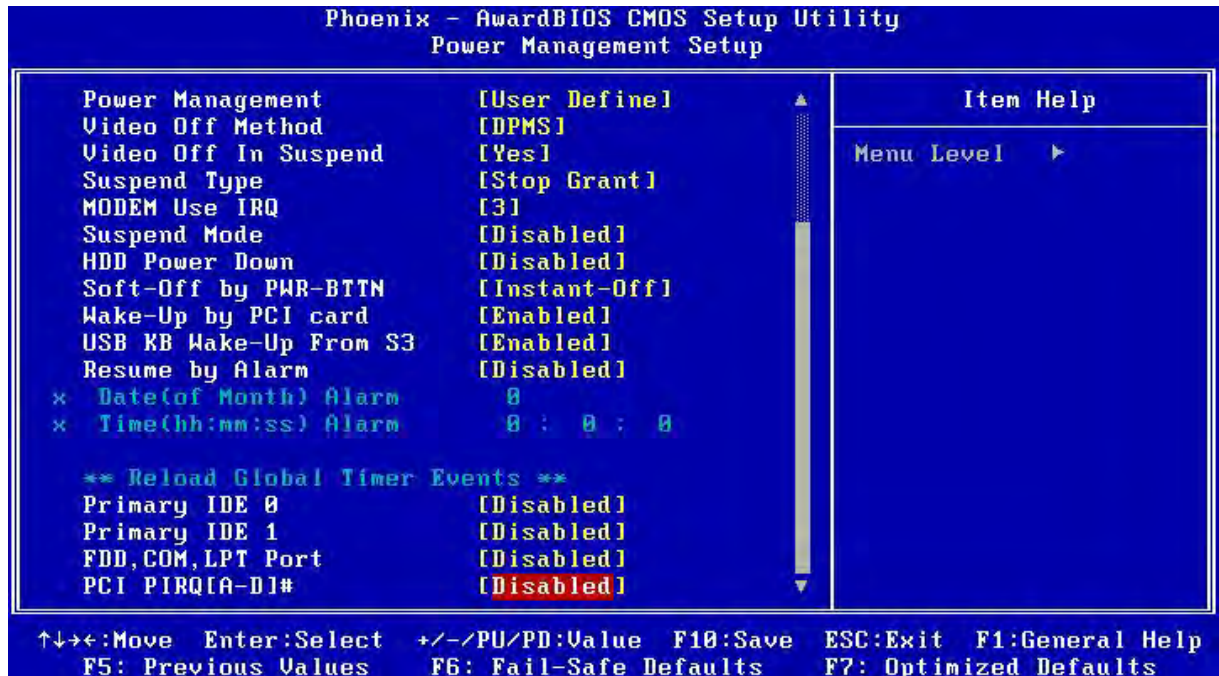
S1: POS – Power On Suspend

No instructions are executed by the processor, RAM contents are preserved

S3: Suspend To RAM (STR), Standby

The current processor context is saved to RAM, the processor itself and most peripherals are switched off. RAM content is preserved by hardware.

Power Management Setup, part 2



When enabled, the Reload Global Timer Events allow restarting the global standby timer when such an event occurs.

PnP/PCI Configurations

Phoenix - AwardBIOS CMOS Setup Utility PnP/PCI Configurations		Item Help
Init Display First	[PCI Slot]	Menu Level ▶
Reset Configuration Data	[Disabled]	
Resources Controlled By	[Auto(ESCD)]	
x IRQ Resources	Press Enter	
PCI/VGA Palette Snoop	[Disabled]	
INT Pin 1 Assignment	[Auto]	
INT Pin 2 Assignment	[Auto]	
INT Pin 3 Assignment	[Auto]	
INT Pin 4 Assignment	[Auto]	
INT Pin 5 Assignment	[Auto]	
INT Pin 6 Assignment	[Auto]	
INT Pin 7 Assignment	[Auto]	
INT Pin 8 Assignment	[Auto]	
** PCI Express relative items **		
Maximum Payload Size	[128]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

For using IRQ on PC/104-Plus set *Resources Controlled by* to **MANUAL**

Select IRQ for PC/104-Plus bus in submenu *IRQ RESOURCES* by setting each needed IRQ from *PCI Device* to *Reserved*

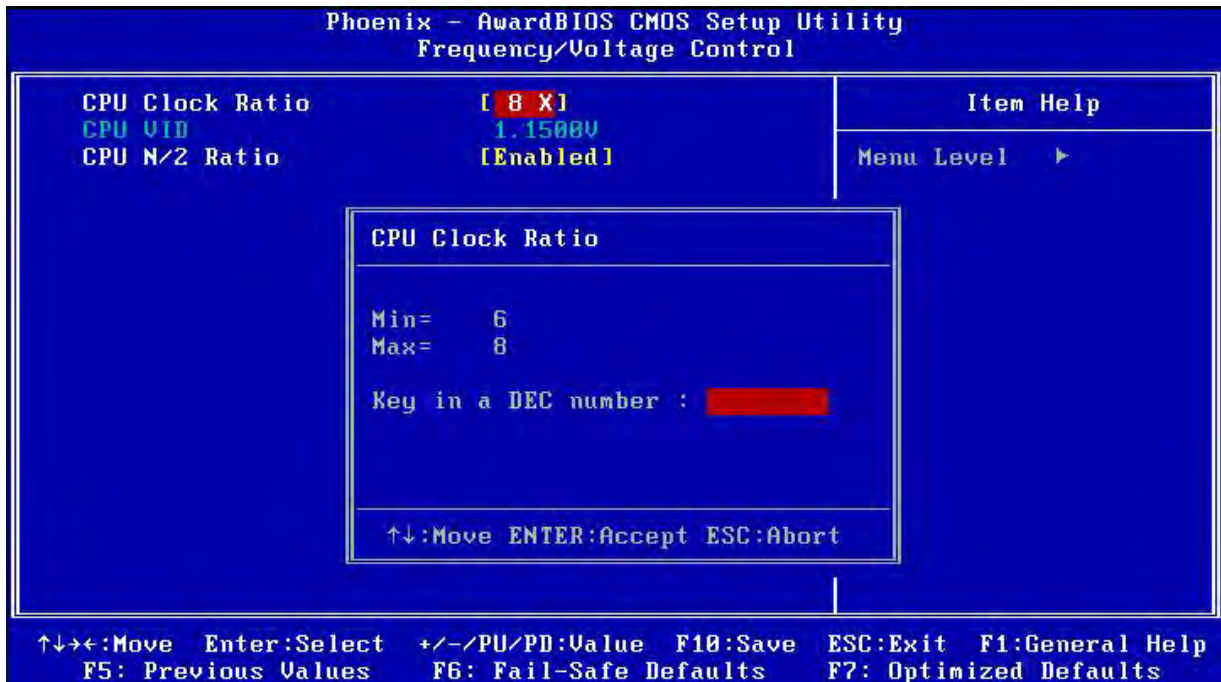


**Note** Depending on IRQ use from onboard resources and other system boards not all IRQ may be used on PC/104-Plus bus. Also reserving too much IRQ for use on PC/104-Plus may result in malfunctions of onboard or other system devices.

Frequency/Voltage Control (Penryn)

Phoenix - AwardBIOS CMOS Setup Utility Frequency/Voltage Control		Item Help
CPU Clock Ratio	[ 8 X]	Menu Level ▶
CPU VID	1.1500V	
CPU N/2 Ratio	[Enabled]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults



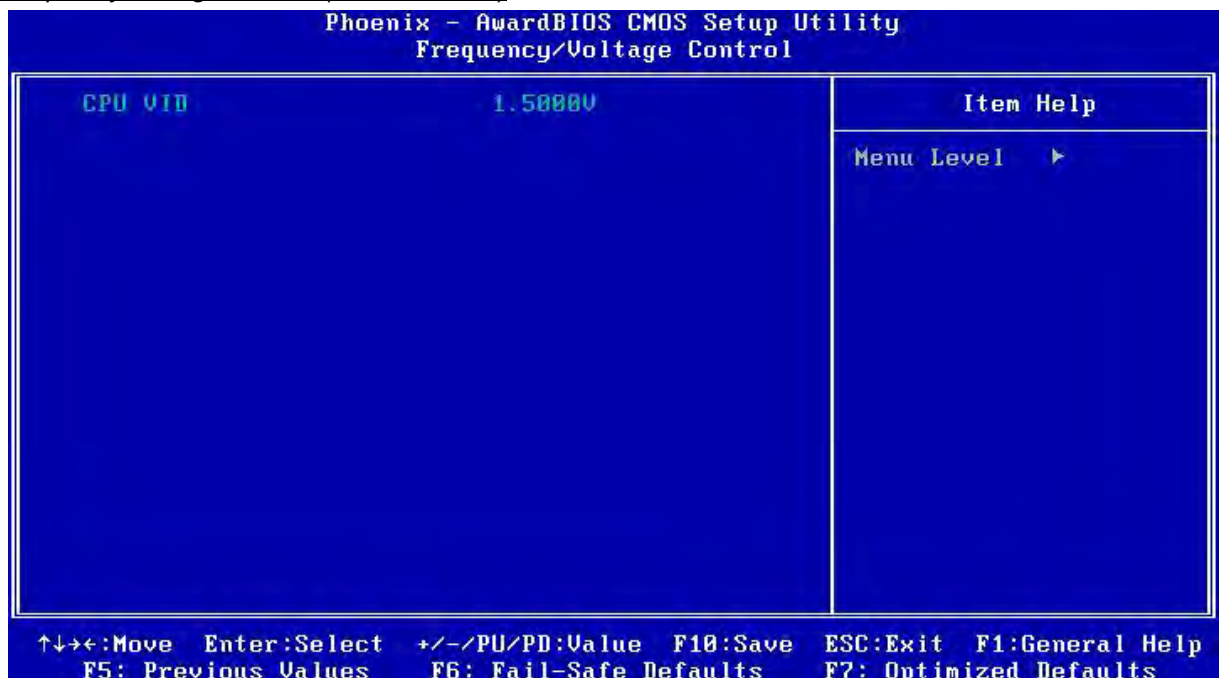
The CPU clock ratio is set by the BIOS, depending on the processor version used. Usually, this is the best setting possible. Changing these values is only recommended for very experienced users and should only be attempted after studying the processor's datasheet.



**Caution**

Use this feature on your own risk.

Frequency/Voltage Control (Celeron M722)



## 4.2 Drivers

Software drivers for Chipset, graphics, Ethernet and audio are available for the Cool XpressRunner-GS45.

These drivers can be downloaded from LiPPERT's website <http://www.lippertembedded.com>.

Follow the installation instructions that come with the drivers.

## 4.3 Programming Examples

The following programming examples are made for a Linux operation system. If other operation systems are used, some header files could be unnecessary or they can have different names.

The "iopl()" function is a Linux specific one, in Windows XP a tool called "porttalk" can be used instead.

Be careful with the interpretation of the "outb" order in our examples:

Linux: "outb(value, address)"

DOS, Windows: "outb(address, value)"

The following example is meant to be compiled using gcc under Linux.

### **LIVE-LED**

Users can program the Live-LED. The cathode of the mounted LED is connected to a GPIO pin of the Super I/O. If the input has ground potential, the LED is on.

The Live-LED (red) can be controlled with bit 3 of I/O port 6CBh (SIO GP13). The BIOS signals with this LED that the POST is in progress. After that, any application program may freely use the LED.

The following program changes the state of the Live-LED.

```
#include <stdio.h>
#include <sys/io.h>           // needed for inb/outb

#define PORT 0x6CB           // Bit 3 of GP1x
#define MASK 0x08           // Address to the GP1x bank

int main()
{
    unsigned char data;
    if (iopl(3))              //get port access permissions (must be root)
    {
        perror("iopl"); return 1;
    }
    data = inb(PORT);         //read GPIOs
    if (data & MASK)          //isolate LED bit (inverse logic!)
    {
        printf("Live LED was off, switching it on.\n");
        outb(data & ~MASK, PORT);
    }
    else
    {
        printf("Live LED was on, switching it off.\n");
        outb(data | MASK, PORT);
    }
    iopl(0);
    return 0;
}
```

## Reading Voltages

It is possible to read out the following power suppliers that are connected to the Super I/O:

1.05 V; 2.5 V; 3.3 V; 5.0 V and 12 V

```
#include <stdio.h>
#include <sys/io.h> // needed for inb/outb

#define EC_INDEX 0x6f0
#define EC_DATA 0x6f1

int main()
{
    unsigned long p2v5, p1v05, p3v3, p5v0, p12v0;

    if (iopl(3)) { // Linux-specific, e.g. DOS doesn't need this
        printf("Failed to get I/O access permissions.\n");
        printf("You must be root to run this.\n");
        return 1;
    }
    printf("\nPress CTRL+C to cancel!\n\n");
    printf("| +1,05 V | +2,5 V | +3,3 V | +5,0 V | +12,0 V |\n");
    printf("|-----+-----+-----+-----+-----|\n");

    while (1)
    {
        outb(0x21, EC_INDEX); // read +1,05 V voltage
        p1v05 = ( inb(EC_DATA) * 2000 ) / 255;
        printf(" | %d.%03d V |", p1v05 / 1000, p1v05 % 1000);

        outb(0x20, EC_INDEX); // read +2,5 V voltage
        p2v5 = ( inb(EC_DATA) * 3320 ) / 255;
        printf(" | %d.%03d V |", p2v5 / 1000, p2v5 % 1000);

        outb(0x22, EC_INDEX); // read +3,3 V voltage
        p3v3 = ( inb(EC_DATA) * 4380 ) / 255;
        printf(" | %d.%03d V |", p3v3 / 1000, p3v3 % 1000);

        outb(0x23, EC_INDEX); // read +5,0 V voltage
        p5v0 = ( inb(EC_DATA) * 6640 ) / 255;
        printf(" | %d.%03d V |", p5v0 / 1000, p5v0 % 1000);

        outb(0x24, EC_INDEX); // read +12 V voltage
        p12v0 = ( inb(EC_DATA) * 1600 ) / 255;
        printf(" | %d.%02d V |\n", p12v0 / 100, p12v0 % 100);

        sleep(1);
    }
    return 0;
}
```

## ***Reading Ambient Temperature***

The Super I/O has an internal temperature sensor, which can be read out. The following code shows an example.

```
#include <stdio.h>
#include <unistd.h>
#include <sys/io.h> // needed for inb/outb

#define EC_INDEX 0x6f0
#define EC_DATA 0x6f1

int main()
{
    signed char ambtemp, start;
    if (iopl(3))
    { // Linux-specific, e.g. DOS doesn't need this
        printf("Failed to get I/O access permissions.\n");
        printf("You must be root to run this.\n");
        return 1;
    }
    outb(0x40, EC_INDEX); //access to start/stop register
    start = 0x01 | inb(EC_DATA);
    outb(start, EC_DATA); //activate monitor mode
    printf("Press CTRL+C to cancel!\n");
    printf("AMBIENT\n");
    while (1)
    {
        outb(0x26, EC_INDEX); //read out ambient temp
        ambtemp = inb(EC_DATA);
        printf("%3d\n", ambtemp);
        fflush(stdout);

        sleep(1);
    }
    return 0;
}
```

## 5. Address Maps

This section describes the mapping of the CPU memory and I/O address spaces.



**Note:** Depending on enabled or disabled functions in the BIOS, other or more resources may be used

### 5.1 Memory Address Map

Address Range (Hex)	Description
00000000-0009FFFF	System
000A0000-000BFFFF	Graphics Controller
000C0000-000DFFFF	PCI-Bus
000E0000-000EFFFF	System
000F0000-000FFFFFF	System
00100000-3BDFFFFFF	System
3BD00000-FEBFFFFFF	PCI-Bus
D0000000-DFFFFFFF	Graphics Controller
E0000000-EFFFFFFF	Resources
FD800000-FDBFFFFFF	Graphics Controller
FDFC0000-FDFDFFFF	Ethernet Controller
FDFE4000-FDFE7FFF	HD-Audio
FDFFC000-FDFFC0FF	SM-Bus
FDFFD000-FDFFD3FF	USB2 Controller
FDFFE000-FDFFE3FF	USB2 Controller
FDFFF000-FDFFFFFF	Ethernet Controller
FEB00000-FEBFFFFFF	Graphics Controller
FEC00000-FEC00FFF	System
FED00000-FED000FF	System
FED00000-FED003FF	Timer
FED13000-FED1FFFF	System
FED20000-FED9FFFF	System
FEE00000-FEE00FFF	System
FFB00000-FFB7FFFF	System
FFB80000-FFBFFFFFF	Firmware Hub
FFF00000-FFFFFFF	System

## 5.2 I/O Address Map

The system chipset implements a number of registers in I/O address space. These registers occupy the following map in the I/O space (depending on enabled or disabled functions in the BIOS other or more resources may be used).

Address Range (Hex)	Description
0000-000F	DMA Controller
0000-0CF7	PCI-Bus
0010-001F	Resources
0020-0021	Interrupt Controller
0040-0043	Timer Controller
0044-005F	Resources
0061-0061	Speaker Control
0062-0063	Resources
0065-006F	Resources
0070-0073	Real Time Clock
0074-007F	Resources
0080-0090	DMA Controller
0091-0093	Resources
0094-009F	DMA Controller
00A0-00A1	Interrupt Controller
00A2-00BF	Resources
00C0-00DF	DMA Controller
00E0-00EF	Resources
00F0-00FF	Math Coprocessor
0274-0277	ISAPnP Data port
0279-0279	ISAPnP Data port
02F8-02FF	Serial Port 2
03B0-03BB	Graphics Controller
03C0-03DF	Graphics Controller
03F8-03FF	Serial Port 1
0400-04BF	Resources
04D0-04D1	Resources
0500-051F	SM-Bus Controller
0680-06FF	Resources
0880-088F	Resources
0A79-0A79	ISAPnP Data port
0D00-FFFF	PCI Bus
EB00-EB0F	SATA Controller 2
EC00-EC0F	SATA Controller 2
ED00-ED03	SATA Controller 2

Address Range (Hex)	Description
EE00-EE07	SATA Controller 2
EF00-EF03	SATA Controller 2
F000-F007	SATA Controller 2
F200-F20F	SATA Controller 1
F300-F30F	SATA Controller 1
F400-F403	SATA Controller 1
F500-F507	SATA Controller 1
F600-F603	SATA Controller 1
F700-F707	SATA Controller 1
F800-F81F	USB Controller
F900-F91F	USB Controller
FA00-FA1F	USB Controller
FB00-FB1F	USB Controller
FC00-FC1F	USB Controller
FD00-FD1F	USB Controller
FE00-FE1F	Ethernet Controller
FF00-FF07	Graphics Controller

### 5.3 Interrupts

IRQ (Bus)	System Resource
0 (ISA)	Timer
3 (ISA)	Serial Port 2
4 (ISA)	Serial Port 1
8 (ISA)	Timer
9 (ISA)	ACPI-conform System
11 (PCI)	SM-Bus Controller
13 (ISA)	Math coprocessor
16 (PCI)	USB Controller – 2937
16 (PCI)	Graphics Controller
18 (PCI)	USB Controller – 2936
18 (PCI)	USB Controller 2 – 293C
19 (PCI)	USB Controller – 2939
19 (PCI)	USB Controller – 2935
19 (PCI)	SATA Controller 1
19 (PCI)	SATA Controller 2
20 (PCI)	Ethernet Controller

21 (PCI)	USB Controller – 2938
22 (PCI)	HD-Audio
23 (PCI)	USB Controller – 2934
23 (PCI)	USB Controller 2 – 293A

#### 5.4 DMA Channels

DMA	System Resource
4	DMA Controller

## 6. Troubleshooting

First steps if the board does not boot:

- Check the status LEDs on the board. Are all voltages properly available?
- Check the power connectors to the board, monitor and additional devices.
- Are all cables plugged on the correct connector and in the correct orientation? The board may not boot if some of the cables are not plugged in correctly!
- Check the power supply. Is the supply voltage correct for the board? If you are not sure, read the manual. Try plugging in a different power supply or multi-meter to check the power a wrong supply voltage can easily FRY a computer and other electrical devices.
- Is your display ok? Is the monitor powered on? Is the monitor's video cable plugged into the video connector? Double-check the brightness and contrast settings. Plug the monitor into another computer if possible to verify the monitor is not the problem.
- Remove all additional devices from the system. Only the processor board, power supply, monitors and the keyboard should remain in the system.
- Assure your cooling measures work correctly and keep the processor at a reasonable temperature.
- If all else has failed, replace the CPU Board itself.
- If system comes up then load at first the OPTIMIZED DEFAULTS in the BIOS setup and reboot.

If you need to send the board to LiPPERT for repair, be sure you get a Return Material Authorization number (RMA) first.

Check also Appendix B (Getting Help).

## Appendix A, Contact Information

### *Headquarters*

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## Appendix B, Getting Help

Should you have technical questions that are not covered by the respective manuals, please contact our support department at [support@lippertembedded.com](mailto:support@lippertembedded.com).

Please allow one working day for an answer!

Technical manuals as well as other literature for all LiPPERT products can be found in the *Products* section of LiPPERT's website [www.lippertembedded.com](http://www.lippertembedded.com). Simply locate the product in question and follow the link to its manual.

### Returning Products for Repair

To return a product to LiPPERT for repair, you need to get a Return Material Authorization (RMA) number first. Please fill in the RMA Request Form at <http://www.lippertembedded.com/service/repairs.html> and send it to us. We will return it to you with the RMA number.

Deliveries without a valid RMA number are returned to sender at his own cost!

LiPPERT has a written Warranty and Repair Policy, which can be retrieved from <http://www.lippertembedded.com/service/warranty.html>

It describes how defective products are handled and what the related costs are. Please read this document carefully before returning a product.

## Appendix C, Further Resources

<http://www.lippertembedded.com>

LiPPERT Embedded Computers' website with news and detailed information.

<http://www.intel.com>

Datasheet of the CPU, Chipset and Ethernet-Controller.

<http://www.smbus.org>

Information about the System Management Bus (SMBus)

<http://www.phoenix.com/en/customer+services/bios/awardbios>

Additional BIOS information.

<http://www.realtek.com.tw/products/productsView.aspx?Langid=1&PNid=24&PFid=28&Level=5&Conn=4&ProdID=135>

Information about the HD-Audio Codec.

## Appendix D, Revision History

Filename	Date	Edited by	Change
TME-PCI104E-GS45-R0V0	2009-02-26	Ulrich Walther	Draft
TME-PCI104E-GS45-R1V0	2009-03-27	PK	Released
TME-PCI104E-GS45-R1V1	2009-08-28	PK	Ordering information corrected.
TME-PCI104E-GS45-R2V0	2009-10-12	Ulrich Walther	Removed remarks for RAM module in chapter troubleshooting. Add programming options and changed/updated BIOS screens in chapter using the module. More details in chapter Module Description.
TME-PCI104E-GS45-R2V1	2009-12-16	Ulrich Walther	More details in chapter Module Description (USB 2.0 Ports, Serial Port).
TME-PCI104E-GS45-R2V2	2010-02-04	Ulrich Walther	Changed MTBF view. Inrush Current. Update table in chapter 3.12
TME-PCI104E-GS45-R2V3	2010-07-29	Ulrich Walther  MS	Update table in chapter 2.1 and 2.2. New chapter 3.9 BIOS Recovery. Changed Top-Pictures. Matching parts / connectors added
TME-PCI104E-GS45-R2V4	2010-09-09	PK	Ch. 1.2: Correct list of available articles
TME-PCI104E-GS45-R2V5	2010-11-11	Ulrich Walther Matthias Fellhauer	Updates in chapter 3.10, 3.11 and 3.13. Ch. 1.2 added 2 GByte models.
TME-PCI104E-GS45-R3V0	2011-08-16	Ulrich Walther / Matthias Fellhauer	New Board-Revision. Changed Top view Pictures. Changed Block Diagramm CH 3.16 added Board specific LEMT functions
TME-PCI104E-GS45-R3V1	2011-12-27	PK	Ch. 1.2: Correct article number of cable set